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Table of Content

A Single Sensor, Single Switch Integrated PFC Buck-Boost Buck Converter Fed BLDC Motor Drive

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Abstract–This paper presents an integrated power factor correction (PFC) buck-boost buck converter based voltage source inverter (VSI) fed brushless DC motor (BLDC) drive using a single voltage sensor. The speed is controlled by controlling the DC bus voltage of the VSI. An electronic commutation of the BLDC motor is used which utilizes a fundamental frequency switching (FFS) of VSI which in-turn offers low switching losses; hence an efficient configuration is realized. A PFC integrated buck-boost buck converter is used as a front-end converter for its operation in a dual-discontinuous conduction mode (DCM) for DC link voltage control and PFC operation. An advantage of fast voltage regulation, with high power factor for wide range of voltage conversion and a zero current switching (ZCS) at turn-on is achieved in this configuration. The proposed drive is designed to achieve an improved power quality at the AC mains for a wide range of speed control with power quality indices under acceptable limits by international power quality standards such as IEC 61000-3-2.

Keywords–BLDC motor drive, buck-boost buck converter, PFC, power quality.

I. INTRODUCTION

Brushless DC (BLDC) motors are becoming popular due to advantages such as high efficiency, high torque/inertia ratio, ruggedness, high energy density, low electro-magnetic interference (EMI) and low maintenance requirement [1, 2]. This motor covers a wide range of applications in household, industrial and medical appliances. The BLDC motor consists of a three phase windings in the stator and permanent magnets on the rotor [3]. It is also known as electronically commuted motor (ECM) as electronic commutation based on the rotor position sensed by Hall Effect position sensor is required for its operation [4, 5]. This motor when fed by a diode bridge rectifier (DBR) with high value of DC link capacitor draws peaky current with crest factor (CF) as high as 3-5. This results in supply current distortion with total harmonic distortion (THD) of the supply current as high as 60-70% and power factor (PF) of the order of 0.8-0.85. These power quality (PQ) indices are not under the acceptable limits by international PQ standards such as IEC 61000-3-2 [6].

Single stage PFC (Power Factor Corrected) converters have been widely used for power quality improvement in BLDC motors [7]. An advantage of reduced losses in the converter stage is achieved due to use of single stage and single switch [8, 9].

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Moreover, simple control scheme is required for single stage as compared to multi-stage converter systems which require two different controls for PFC and voltage regulation [10]. An integrated PFC buck-boost buck configuration is used in this paper which utilizes a single switch and has following advantages [11]:

1.Low losses in single stage, single switch configuration.
2.Fast voltage regulation for improved dynamic performance.
3.PFC and improved power quality at AC mains over a wide voltage conversion ratio.
4.Switch turn on at zero current (ZCS- Zero Current Switching) for reduced losses in switch.

Total losses in a BLDC drive system consists of losses in PFC converter (P_{loss_conv}), losses in VSI (P_{loss_inv}) and losses in BLDC motor (P_{loss_motor}) itself as shown in equation (1). The inherent losses in BLDC motor can't be minimized due to the finite resistance of the stator's windings, frictional and magnetic losses. Moreover, the switching losses in AC-DC converter depends on the switching frequency which has to be kept high of the order of 50kHz for the effective operation of converter and reducing the size of inductors. Hence switching frequency of converter also can't be modified. But, the switching losses in the VSI can be reduced by using an electronic commutation of the BLDC motor which utilizes a fundamental frequency switching of the VSI.

$$P_{loss} = P_{loss\_conv} + P_{loss\_inv} + P_{loss\_motor} \quad (1)$$

$$P_{loss\_inv} = P_{loss\_switching} + P_{loss\_conduction} \quad (2)$$

As shown in equation (2) the switching losses and conduction losses of IGBT's in the VSI combines to give overall losses. Switching losses, which shares a major portion of total losses in the VSI, are proportional to the square of switching frequency which is reduced from 10-20kHz (for PWM operation) to few Hz's and the corresponding reduction in switching losses.

The PFC converter can be operated in CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) of operation [8, 9]. A CCM operation uses a current multiplier approach which requires sensing of input voltage, input current and DC link voltage, hence requires three sensors. A reduced sensor configuration of BLDC motor drive is achieved by DCM operation of PFC converter which uses a voltage follower scheme for a single voltage sensor operation for PFC and DC link voltage control. But these advantages are achieved at the cost of higher stresses on the PFC converter switch; hence the evaluation of current and voltage stress become essential to determine the feasibility of the proposed BLDC motor drive.

II. PROPOSED INTEGRATED PFC BUCK-BOOST BUCK CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BLDC motor system using an integrated PFC converter which is a combination of a PFC buck-boost and a buck converter. The speed control of BLDC motor is achieved by controlling the DC link voltage of the VSI [12]. This type of control provides a freedom to operate VSI in fundamental frequency switching mode for achieving an electronic commutation of the BLDC motor. This also reduces the switching losses many times as compared to the PWM (Pulse Width Modulation) switching. The performance of the proposed drive is evaluated for speed control over a wide range with improved power quality (i.e. high power factor and low supply current distortion) at the AC mains, satisfying the guidelines of IEC 61000-3-2. Performance is also evaluated for varying supply voltage to demonstrate the behavior for practical supply conditions. Moreover, voltage and current stress on the switch are also evaluated to determine the feasibility of proposed BLDC motor drive.

III. OPERATING PRINCIPLE OF AN INTEGRATED PFC BUCK-BOOST BUCK CONVERTER

The integrated PFC buck-boost buck converter is designed to operate in dual DCM such that currents in input inductor L_i and output inductor L_o become discontinuous in a switching period. Figs. 2 (a-d) and Fig. 2(e) show four different modes of operation and waveform of inductor currents and capacitor voltages during a single switching period respectively. Different modes of operation are described below.

Mode I: In this mode, switch S_w is turn on to charge the input inductor L_i with diode D_1 remaining in forward biased position to close the input side circuit as shown in Fig. 2(a). The current in input inductor L_i increases which rate of increase depends upon the instantaneous input voltage applied. The energy stored in intermediate capacitor C_1 starts discharging through switch S_w via output inductor L_o and diode D_3 to charge the DC link capacitor, C_d. Diodes D_2 and D_4 remain reversed biased during this mode and hence no current flows through them. As shown in Fig. 2(e), inductor's currents i_{Li} and i_{Lo} increase and the voltage across intermediate capacitor V_{C1} decreases in this mode.

Mode II: In this mode of operation as shown in Fig. 2(b), switch S_w is turned off; hence inductors L_i and L_o discharge their stored magnetic energy to charge the intermediate capacitor C_1 and DC link capacitor C_d. Diode D_3 remains in reverse blocking while diodes D_1, D_2 and D_4 conduct for achieving a required closed loop for energy transfer between inductors and capacitors. Voltage across intermediate capacitor (V_{C1}) starts increasing till the energy stored in inductor L_i becomes zero. At the end of this mode, input inductor current i_{Li} becomes zero and enters into DCM while still some energy is left in output inductor L_o due to its higher value of time constant ($\tau_o=L_oC_d$).

Mode III: In this mode, switch S_w remains in off position and input side is not supplying any energy to the converter

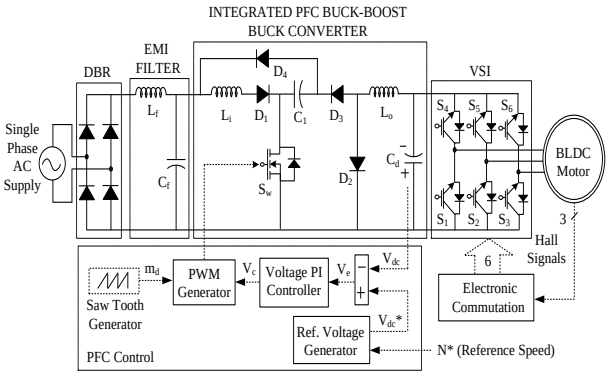

Fig. 1: Proposed Integrated PFC buck-boost buck converter fed BLDC motor Drive

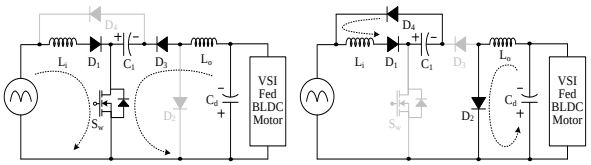

Fig. 2(a): Mode I

Fig. 2(b): Mode II

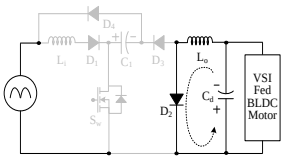

Fig. 2(c). Mode III

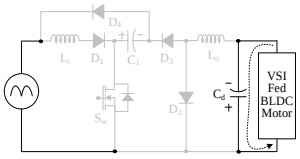

Fig. 2(d). Mode IV

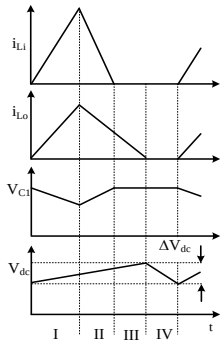

Fig. 2(e). Waveforms

Fig. 2: Different modes of operation of integrated PFC buck-boost buck converter

as shown in Fig. 2(c). Only output side inductor L_o transfers all of its energy to charge the DC link capacitor, hence the voltage V_{dc} continues to increase, while the voltage across the intermediate capacitor C_1 remains constant in this mode. At the end of this mode, inductor L_o is completely discharged and current i_{Lo} becomes zero.

Mode IV: As shown in Fig. 2(d) there is no energy left in input inductor L_i and output inductor L_o and hence converter enters into a dual DCM operation. The DC link capacitor supplies the required energy to the load and voltage across it reduces as shown in Fig. 2(e). The intermediate capacitor C_1 remains charged with its highest possible voltage. This mode is completed with the end of switching period and the complete cycle is repeated for the next switching state.

IV. DESIGN OF AN INTEGRATED PFC BUCK-BOOST BUCK CONVERTER

The design of integrated PFC buck-boost buck converter consists of designing and selection of optimum values of boost inductor (L_i), output filter inductor (L_o), intermediate

(bulk) capacitor (C_1) and DC link capacitor (C_d). The design of converter is based on the following specifications with BLDC motor rating given in Appendix.

P_m (Rated Power of BLDC motor) = 377W, P_o (Rated power of converter to be designed) = 450W, V_S (Supply RMS voltage) = 220V, V_{dcmax} (Rated DC link voltage) = 310V, V_{dcmin} (Minimum DC link voltage) = 70V, V_{dc} (Designed Value of DC link voltage which is average of maximum and minimum DC link voltage) = 190V, ΔV_{C1} (Permitted ripple voltage in intermediate capacitor) = 10% of V_{C1}, ΔV_{dc} (Permitted ripple voltage in DC link capacitor) = 1% of V_{dc}, f_S (Switching frequency) = 45kHz, f_L (Power frequency) = 50Hz.

The input average voltage after the DBR (rectified voltage) is calculated as [10],

$$V_{in} = \frac{2\sqrt{2}V_S}{\pi} = \frac{2\sqrt{2}\times 220}{\pi} = 197.98V \approx 198V \quad (3)$$

The output voltage, V_{dc} of given integrated PFC converter which is of buck-boost type is given as [9],

$$V_{dc} = \frac{D}{(1\text{-}D)} V_{in} \quad (4)$$

where D is the duty ratio.
From equation (3), the nominal duty ratio, D_{nom} corresponding to designed value of DC link voltage is calculated as,

$$D_{nom} = \frac{V_{dc}}{V_{dc}+V_{in}} = \frac{190}{190+198} = 0.4896 \quad (5)$$

The critical value of input inductor L_{icrit} to operate at boundary of CCM and DCM is given and calculated as [9],

$$L_{icrit} = \frac{V_{in}D_{nom}}{2f_S I_{in}} = \frac{198\times 0.4896}{2x45000\times(450/198)} = 473.93\mu H \quad (6)$$

The value of input inductor L_i is to be selected such that $L_i < L_{icrit}$ for DCM operation. Hence value of L_i is selected as 200 µH.
Similarly the critical value of output inductor L_{ocrit} is expressed as [9],

$$L_{ocrit} = \frac{V_o(1\text{-}D_{nom})}{2f_S I_o} = \frac{190\times(1\text{-}0.4896)}{2x45000\times(450/190)} = 454.94\mu H \quad (7)$$

Hence the value of magnetizing inductance L_o to operate in DCM is selected such that $L_o < L_{ocrit}$, hence a value of L_o is chosen as 200 µH.
The value of intermediate (bulk) capacitor C_1 is calculated as [9],

$$C_1 = \frac{V_{dc}D_{nom}}{f_s R_L \Delta V_{C1}} = \frac{190\times 0.4896}{45000\times(190^2/450)\times 0.1\times(398)} = 664.4nF \quad (8)$$

where the voltage V_{C1} across capacitor C_1 is sum of input and DC link voltage (i.e. $V_{C1} = V_{in} + V_{dc}$). Hence, value of intermediate (bulk) capacitor C_1 is selected as 500nF.
The value of DC link capacitor is calculated as [9],

$$C_d = \frac{I_{dc}}{2\omega_L \Delta V_{dc}} = \frac{(P_o/V_{dc})}{2\omega_L \Delta V_{dc}} = \frac{(450/190)}{2\times 314\times 0.01\times 190} = 1985\mu F \quad (9)$$

where I_{dc} is DC link current.

Hence the value of DC link capacitor is taken as 2200 µF.
To avoid the EMI problems due to high switching frequency reflection in the supply, an EMI filter is designed which is a LC filter with maximum value of filter capacitance C_{max} is given as [13],

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan(\theta) = \frac{(P_o/V_s)}{\omega_L V_{peak}} \tan(\theta) = \frac{(450\sqrt{2}/220)}{314\times 311} \tan(3^\circ) = 341.5nF \quad (10)$$

where I_{peak} and V_{peak} are the peak input current and peak input voltage respectively and θ is the displacement angle.

The value of filter capacitance C_f is selected lower than C_{max}, hence the value of C_f is selected as 330nF.

The expression for the calculation of filter inductance L_f is given as [13],

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} = \frac{1}{4\pi^2 (4500)^2 \; ?\; 30?\; 0^{-9}} = 3.79mH \quad (11)$$

where f_c is the cut-off frequency such that $f_c = f_s/10$ [13].

Hence an inductance L_f of the order of 4mH is selected for input EMI filter.

V. CONTROL OF PROPOSED PFC CONVERTER FED BLDC MOTOR DRIVE

The control of an integrated PFC buck-boost-buck converter fed BLDC motor drive is classified into two controls of PFC converter and BLDC motor as follows.

A. Control of PFC Converter

A voltage follower approach for PFC and DC link voltage control is utilized for an integrated PFC buck-boost buck operating in dual DCM. In this mode of operation, it acts as an inherent power factor pre-regulator utilizing a single voltage sensor. The reference voltage V_{dc}* is obtained by multiplying the reference speed (N*) with the motor's voltage constant (k_v) as,

$$V_{dc}^* = k_v N^* \quad (12)$$

Now, this reference DC link voltage (V_{dc}*) is copmpared with sensed DC link voltage (V_{dc}) to generate a voltage error which is to be given to the voltage PI (Proportional-Integral) controller for necessary control action. The error voltage (V_e) is at any time instant '*k*' is given as,

$$V_e(k)=V_{dc}^{*}(k)-V_{dc}(k) \quad (13)$$

The voltage error obtained in equation (13) is given to the PI controller whose controlled output V_c is given as,

$$V_c(k)=V_c(k-1)+K_p\{V_e(k)-V_e(k-1)\}+K_iV_e(k) \quad (14)$$

where $V_c(k)$ and $V_c(k-1)$ represent the controller output at k^{th} and $k\text{-}1^{th}$ sampling instant and K_p and K_i are the proportional and integral gains of the PI controller.

The controlled output V_c as given in equation (14), is compared with a high frequency saw-tooth waveforms to generate PWM signals to be given to the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) of the PFC converter for the required voltage control.

B. Control of BLDC Motor: Electronic Commutation

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical DC current is drawn from the DC link capacitor for 120^0 and placed symmetrically at the centre of each phase. A Hall-Effect position sensor is used to sense the rotor position on a span of 60^0; which is required for the electronic commutation of BLDC motor. The conduction states of two switches (S_1 and S_4) are shown in Fig. 3. A line current i_{ab} is drawn from the DC link capacitor which magnitude depends on the applied DC link voltage (V_{dc}), back emfs (e_{an} and e_{bn}), resistances (R_a and R_b) and self and mutual inductance (L_a, L_b and M) of the stator windings. Table 1 shows the different switching states of the VSI feeding a BLDC motor based on the Hall Effect position signals (H_a-H_c).

VI. PERFORMANCE EVALUATION OF THE PROPOSED BLDC MOTOR DRIVE

The performance of the proposed BLDC motor drive is evaluated on the basis of PQ indices such as PF (Power Factor), DPF (Displacement Power Factor), DF (Distortion Factor), CF (Crest Factor) and THD (Total Harmonic Distortion) of supply current at AC mains. Various performance indices such as supply voltage (V_s) and supply current (i_s) are analyzed for power quality assessment. Indices such as DC link voltage (V_{dc}), speed (N), electromagnetic torque (T_e), stator current (i_{sa}), inductors current (i_{Li} and i_{Lo}) and intermediate capacitor's voltage (V_{C1}) are evaluated for demonstrating the proper functioning of BLDC motor and PFC converter. An improved power quality over a wide range of speed control of BLDC motor is achieved. The proposed drive is also evaluated for supply voltage variation to demonstrate the performance for practical supply situations. Moreover, switch stresses (v_{sw} and i_{sw}) are also analyzed for proper selection of switch and heat sink design.

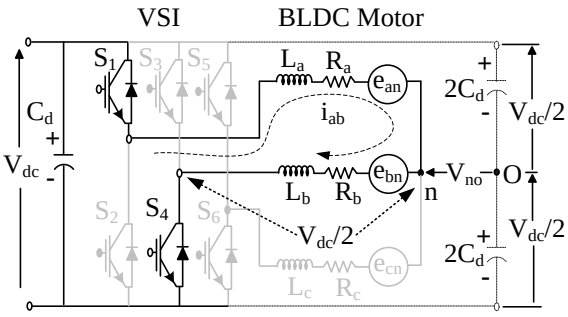

Fig. 3: A BLDC motor fed by a VSI showing the current flow when two switches S_1 and S_4 are in on state

Table 1: Switching states of VSI based on hall effect position sensor signal

θ^o	*Hall Signals*			*Switching States*					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

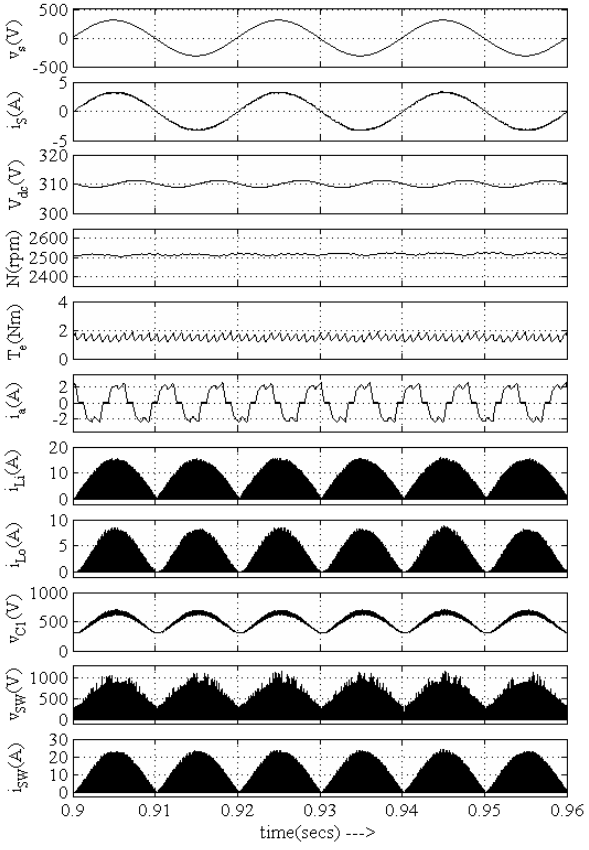

Fig. 4: Steady state behavior of the proposed drive at rated load on BLDC motor.

Fig. 4 shows the steady state behavior of the proposed drive system on a magnified scale. As shown in the figure, supply current (i_s) is in phase with supply voltage (v_s) and is sinusoidal in nature which shows a near unity DPF and near unity DF, hence a near unity PF (PF=DF*DPF) is obtained at the AC mains. The DC link voltage (V_{dc}) is maintained at the rated value of 310 V which corresponds

to the speed of 2500 rpm (N) of BLDC motor. An electromagnetic torque of the order of 1.7 Nm is achieved with a limited ripple in the torque (T_e) and stator current (i_a) showing the proper operation of BLDC motor. A discontinuous current is achieved in input and output inductor (i_{Li} and i_{Lo}), whereas the intermediate capacitor's voltage (V_{C1}) remains in continuous conduction for a switching period. This verifies the dual DCM operation of an integrated PFC buck-boost buck converter. As shown, in this figure, the peak voltage (v_{sw}) and current (i_{sw}) stress of the order of 900 V/22 A is achieved on the PFC converter switch. Table 2 shows the various performance indices for speed control of BLDC motor by controlling the DC link voltage from 70V (buck mode) to 310V (boost mode). A high power factor of the order of 0.99 and THD of supply current below 5% is obtained for a wide voltage conversion ratio (wide speed control) satisfying the acceptable limits of international PQ standard IEC 61000-3-2. A zero current switch turn on phenomena (ZCS turn on) is obtained as shown in Fig. 5. This is achieved to due to operation of PFC converter such that the switch voltage (V_{sw}) becomes zero during the turn-on of PFC converter switch as shown in Mode-III and Mode-IV in Fig.2. This reduces switching losses in a PFC converter due to zero current appearing across the switch during the turn-on.

Table 2: Performance of integrated PFC buck-boost buck converter fed BLDC motor drive under speed control

V_{dc} (V)	Speed (rpm)	THD of I_s (%)	DPF	PF	I_s (A)
70	260	3.31	0.9999	0.9994	0.5118
90	440	3.05	1	0.9995	0.643
110	640	2.94	1	0.9996	0.7758
130	820	2.82	1	0.9996	0.9115
150	1030	2.77	0.9999	0.9995	1.048
170	1200	2.56	0.9998	0.9995	1.192
190	1460	2.43	0.9997	0.9994	1.339
210	1610	2.39	0.9997	0.9994	1.478
230	1780	2.37	0.9995	0.9992	1.63
250	1970	2.14	0.9993	0.9991	1.767
270	2100	1.78	0.9992	0.999	1.926
290	2350	1.74	0.9988	0.9986	2.087
310	2520	1.64	0.9985	0.9984	2.218

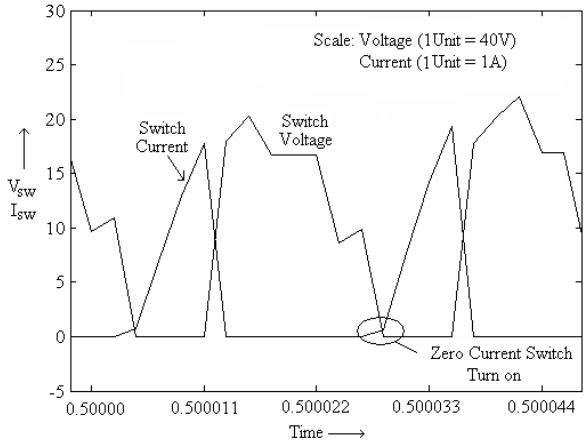

Fig. 5: Switch voltage and current showing the zero current switch turn on phenomenon.

Fig. 6 shows the dynamic behavior of the proposed BLDC motor drive system during speed control. As shown in this figure, the BLDC motor is started at DC link voltage of 100V and the speed is varied corresponding to change in DC link voltage from 100V to 300V at 0.35s. A smooth control of DC link voltage (V_{dc}) is achieved i.e. smooth control of speed limited transients in supply and stator current; which demonstrates the proper functioning of control loop. A rate limiter is used to limit the sudden change in parameters like voltage or current. Table 3 shows the evaluated performance for supply voltage variation from 170V-270V to demonstrate the behavior of proposed drive for practical supply condition. PQ indices obtained are within the recommended limits of IEC 61000-3-2.

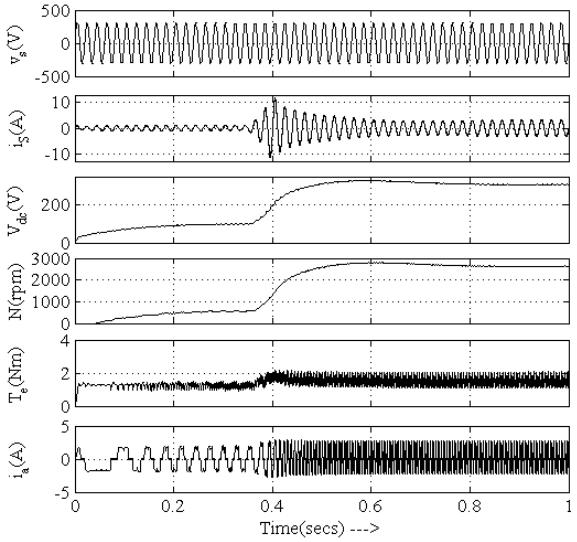

Fig. 6: Dynamic behavior of proposed drive during starting and speed control

Table 3: Performance of proposed BLDC motor drive under varying supply voltage

V_s (V)	THD of I_s (%)	DPF	PF	I_s (A)	CF
170	1.41	0.9999	0.9953	2.805	1.414
180	1.47	0.9999	0.9964	2.634	1.414
190	1.52	0.9999	0.9971	2.505	1.414
200	1.58	0.9999	0.9978	2.383	1.414
210	1.61	0.9999	0.9982	2.305	1.414
220	1.64	0.9999	0.9984	2.218	1.414
230	1.72	0.9999	0.9987	2.14	1.414
240	1.85	0.9998	0.9991	2.08	1.414
250	1.94	0.9998	0.9992	1.985	1.414
260	2.11	0.9998	0.9993	1.892	1.414
270	2.34	0.9997	0.9993	1.844	1.414

Table 4: Voltage and current stresses under different loading

Load (%)	v_{sw} (V)	i_{peak} (A)	i_{rms} (A)
10	900	13	0.3974
20	900	14	0.53
30	900	15	0.6647
40	900	16	0.7954
50	900	17	0.981
60	900	18	1.16
70	900	19	1.215
80	900	20	1.27
90	900	21	1.374
100	900	22	1.52

Harmonic spectra of supply current for DC link voltage of 310V and 70V are shown in Fig. 7(a) and Fig. 7(b) respectively. The THD of supply current obtained is well maintained below 5% for both cases. Stresses on the PFC converter's switch in term of peak voltage stress (V_{sw}), peak current stress (i_{peak}) and rms value of current (i_{rms}) flowing through switch are evaluated for different loading on BLDC motor and is tabulated in Table 4. Fig. 8 (a) and Fig. 8 (b) show the PF and THD of supply current with respect to DC link voltage and supply voltage respectively. A unity power factor for both mentioned cases and THD of supply current below 5% are obtained for the complete range of DC link voltage and supply voltage variation. Peak current and voltage stress are used for proper rating selection of switch, whereas rms current is used for heat sink design. The performance of the proposed drive seems to be satisfactory in all aspects and is a good solution for a low cost, high efficiency BLDC motor drive system.

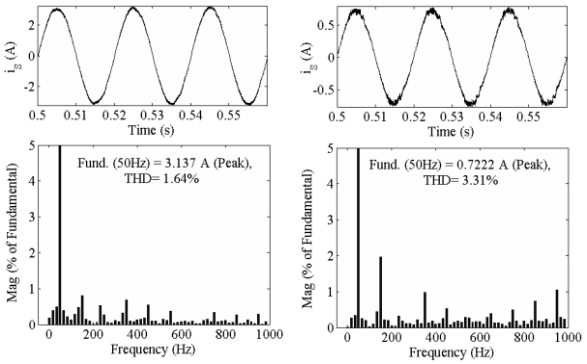

Fig. 7(a) Fig. 7(b)

Fig. 7: Harmonic spectra of supply current at rated conditions with DC link voltage as (a) 310V and (b) 70V.

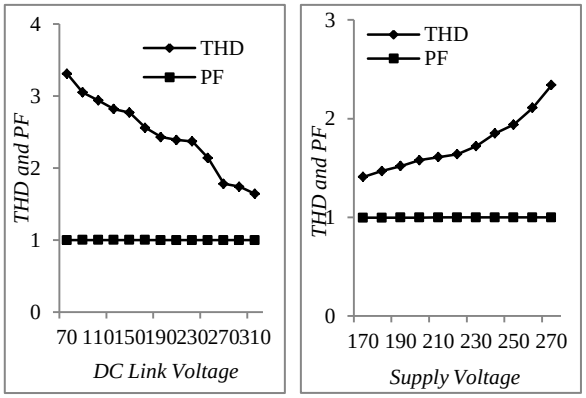

Fig. 8(a) Fig. 8(b)

Fig. 8: Variation of THD of supply current and PF at AC mains with (a) DC link voltage and (b) supply voltage.

VII. Conclusion

An integrated PFC buck-boost buck converter has been proposed for BLDC motor drive. The speed of BLDC motor has been controlled by varying the DC link voltage of VSI using a single voltage sensor. The PFC converter has been designed to operate in dual DCM operation for PFC and DC link voltage control. A zero current switch turn-on of PFC converter has been implemented for enhancing the efficiency of proposed drive. A fundamental frequency switching of VSI has been used for reducing the switching losses in VSI. The performance of the proposed drive has been evaluated for a wide range of speed control and supply voltage variation with PQ indices obtained within the acceptable limits by international PQ standard IEC 61000-3-2. The proposed BLDC motor drive is a recommended solution for many low power applications with speed control and improved power quality at the AC mains.

Appendix

BLDC Motor Rating: 4 poles, P_{rated} (Rated Power) = 0.5 hp (377W), V_{rated} (Rated DC link Voltage) = 310 V, T_{rated} (Rated Torque) = 1.2 Nm, ω_{rated} (Rated Speed) = 3000 rpm, K_b (Back EMF Constant) = 78 V/krpm, K_t (Torque Constant) = 0.74 Nm/A, R_{ph} (Phase Resistance) = 14.56 Ω, L_{ph} (Phase Inductance) = 25.71 mH, J (Moment of Inertia) = 1.3x10-4 Nm/s^2.

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BIOGRAPHIES

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Isolated Bridgeless Cuk Converter with Improved Power Quality for Welding Power Supply

Swati Narula [1] G. Bhuvaneswari [2] Bhim Singh [3]

Abstract– This paper deals with a new single-phase bridgeless AC-DC converter for AWPS (Arc Welding Power Supply) with an ability to improve the power factor at AC mains. The PFC (Power Factor Correction) converter is based on high frequency isolated Cuk converter topology. The conduction losses are reduced by eliminating the DBR (Diode Bridge Rectifier) in classical converter topology. The proposed converter topology is designed to operate in DCM (Discontinuous Conduction Mode) for simple control and to minimize the EMI (Electromagnetic Interference). The DCM operation also facilitates to achieve a unity power factor at AC mains. This converter regulates constant voltage at the output in the range of welding currents and inherent parametrical short-circuit current limit to improve the weld bead quality. The dynamic and steady state responses of the proposed AC-DC converter are included to validate the capability of converter for welding power supply.

Keywords–Bridgeless rectifier, Cuk converter, high frequency transformer, power factor correction, power quality, total harmonic distortion, welding power supply

I. INTRODUCTION

Now-a-days welding power supplies with active PFC (Power Factor Correction) are preferred to meet harmonics regulations and standards as per IEC 61000-3-2 [1]. Significant efforts have been made in developing PFC based converters to reduce the harmonics contents in AC Mains [2-3]. Generally, PFC based power supplies consist of a DBR followed by a high frequency transformer of the DC-DC converter [4]. However, the efficiency of this conventional PFC converter is low because of the conduction losses caused by the diode bridge. Moreover in high power applications, the high conduction loss in the DBR degrades the overall system efficiency. Moreover, the diodes may be destroyed due to the heat generated within the diode bridge. The bridgeless topologies discussed in [5-7], have been implemented as boost rectifier to achieve high power factor. But it suffers from the drawbacks such as high inrush current, lack of current limiting during overload conditions and no galvanic isolation. In proposed bridgeless PFC converter, the current flows through a minimum number of switching devices which in turn minimizes the conduction losses. Furthermore, its cost is also reduced [8-9].

In order to stabilize the arc length in welding power supply, a welding power source with constant voltage output characteristic is usually preferred [10]. Initially, the electrode is too cold to emit electrons to establish the arc. Generally, an arc is initiated by scratching or touching the electrode on the base metal, which causes a short-circuit condition while the load current should be controlled to a desired value [11-12].

Even during normal welding condition, there is a possibility that the electrode comes into contact with the work-piece which arises a short circuit condition. High short circuit current results in increased spatter generation and poor weld quality [13]. This makes arc welding a stochastic process and it becomes indispensable to analyze the dynamic characteristics of the entire welding process. This paper presents a bridgeless Cuk converter based AWPS. The proposed topology consists of two isolated Cuk converters, one conducting for each half line period of the AC mains voltage. The Cuk converter has several commendable features such as reduced EMI, less conduction losses, inherent protection against inrush current, low switching current ripple, easy implementation of galvanic isolation and high overall conversion efficiency [14-16].

The short circuit protection has been incorporated in proposed power supply which appreciably improves the weld bead quality. The double loop control scheme aids in limiting the output current to 1.25 p.u. even during short circuit conditions. Moreover, eliminating the DBR at the front end reduces the conduction losses. It offers improved thermal utilization of the semiconductor switches as switch rms current is bifurcated into two switches and being a single stage PFC configuration, it minimizes the complexity of the system. Furthermore, the high frequency isolation leads to an excellent voltage control and safe operation, desired for the welding equipment. Besides, input current shaping is inherent in Cuk converter operating in DCM (Discontinuous Conduction Mode) [17]. Therefore, the proposed converter is made to operate in DCM and the duty cycle is mainly decided by the DC output voltage follower. The design, control and modeling of the single phase bridgeless Cuk converter using PWM (Pulse-Width Modulation) are carried out using MATLAB-Simulink environment developed by MathWorks [18]. In order to illustrate the performance of proposed topology, some design aspects are discussed in relation to different loads and supply voltage conditions during welding process.

II. SYSTEM CONFIGURATION

The proposed bridgeless Cuk converter based AWPS is shown in Fig. 1. This topology is formed by connecting two isolated Cuk converters in such a way that one conducts with a positive half cycle of input AC mains while the other one with a negative half cycle of input AC mains. It comprises of AC mains, Cuk converters, high frequency rectifier, output filter and welding load. High frequency isolation provides improved voltage control and

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safety of welding load equipment. The high operating frequency also results in a significant reduction in the dimensions and mass of the welding power supply compared to the conventional ones which operate at the mains frequencies.

A single stage isolated bridgeless Cuk AC-DC converter consists of two conversion processes, one during positive half cycle and the other one during negative half cycle. For the positive half cycle switch S_1 is turned on and for the negative half cycle switch S_2 conducts.

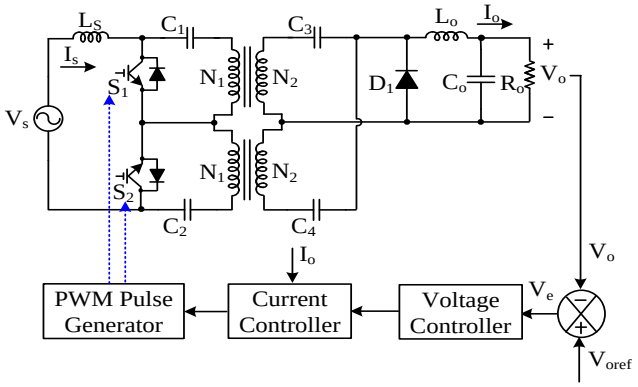


Fig.1: Circuit configuration of isolated bridgeless Cuk converter based AWPS.

Fig. 2 shows the operating modes of bridgeless Cuk converter for positive and negative half cycles of the supply voltage Referring to Fig. 2a, during the positive half-line cycle of input AC mains voltage, S_1, C_1, C_3, D_1 and body diode of switch S_2 are conducting, which connects the input ac source to the output welding load, R_o. Similarly, during the negative half cycle, S_2, C_2, C_4, D_1 and body diode of switch S_1 conduct as shown in Fig. 2b. Thus there is a reduction in the current stress on the power switches as each one is operating for half of the cycle only. These two switches can be driven from the same control signal which adds simplicity to the circuit. The output inductor, L_o and capacitor, C_o reduces the output voltage ripple.

During positive half cycle of the supply voltage, the switch S_1 is turned on and the diode, D_1 remains reversed biased as shown in Fig. 2a(i). When switch S_1 is turned off and diode D_1 becomes forward biased. The inductor freewheels its stored energy to the load as presented in Fig. 2a(ii). In Fig. 2a(iii), the inductor enters into the DCM and the switch S_1 and the diode D_1 remain turned off during this period. Similarly, the operation of the proposed converter during negative half cycle of the supply voltage is shown in Fig. 2b(i)-(iii).

PWM (Pulse Width Modulation) technique has been used to ensure DCM operation of the proposed converter. The double loop control has been implemented to avoid the problems such as spattering, instability of arc length, poor weld bead quality etc.

The sensed output DC voltage, V_o is compared with the reference DC voltage, V_{oref} then the generated voltage error, V_e is given to PI (Proportional-Integral) voltage controller. The output of the PI voltage controller acts as a reference current signal for the PI current controller. This reference current is compared with the output current which generates the error and this error is given to PI current controller to restrict the output current in the desired limit. The output of current controller is compared with ramp signal to generate gating pulses for Cuk converters.

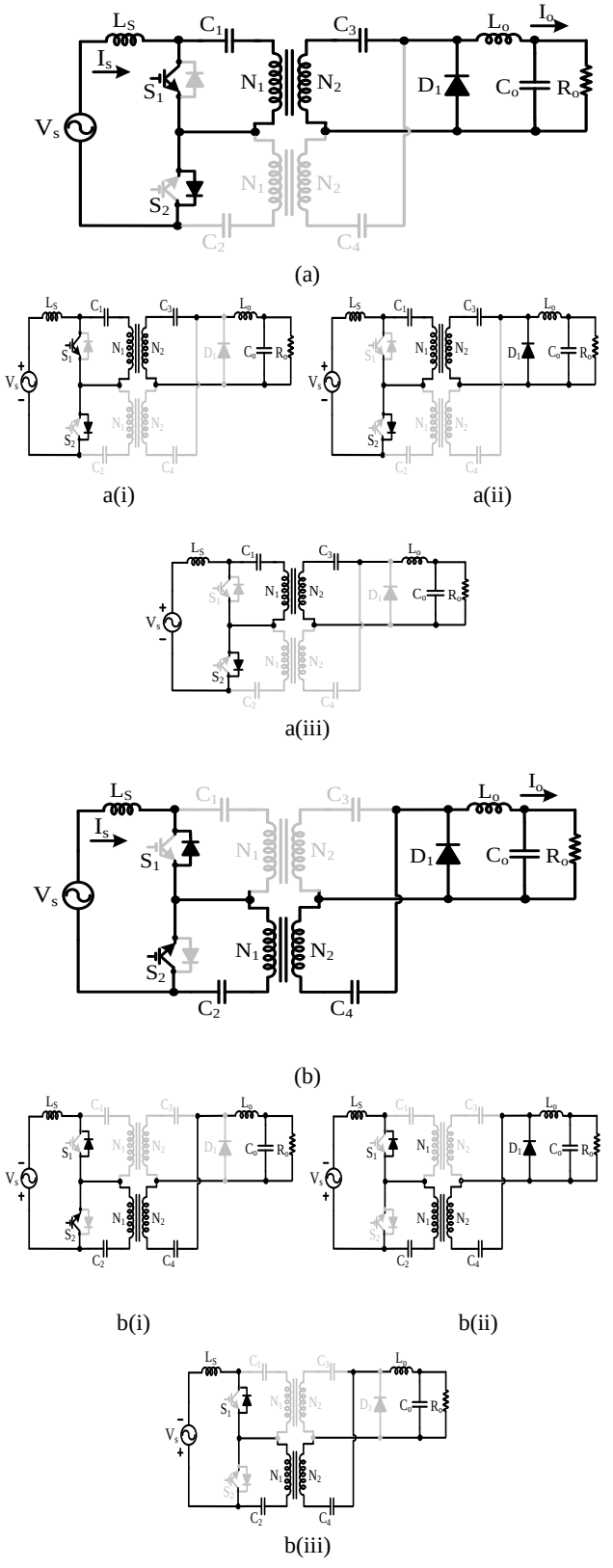


Fig.2a: Bridgeless Cuk converter based AWPS operation during positive half cycle 2a (i)-(iii).
2b: Bridgeless Cuk converter based AWPS operation during negative half cycle 2b (i)-(iii).

III. Design Example Of Proposed AWPS

In this section, the design and analysis of the proposed single phase welding power supply have been discussed in detail. For the sake of simplicity, a single module of isolated Cuk converter has been considered and a pure resistance is taken as a welding load. Due to the symmetry of the proposed circuit, the circuit is analyzed during positive half cycle of the input voltage only. For analysis purposes, the supply voltage, v_{in} is considered to be a constant within each switching cycle; this is because the line frequency f(=50 Hz) is much lower than the switching frequency f_s (=50 kHz).

In steady state condition, the average voltages across the primary and secondary windings of the high frequency transformer and inductors L_S and L_o and the transformer primary and secondary windings are equal to zero. Thus,

$$V_1(avg) = V_2(avg) = V_{Ls}(avg) = V_{Lo}(avg) \quad (1)$$

$$V_{sav} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2}*220}{\pi} \cong 198\ V \quad (2)$$

By applying the constant volt-second relationship, the voltage conversion ratio of the isolated Cuk converter can be derived to calculate the turns ratio of the high frequency transformer operating at 50 kHz.

For an isolated Cuk converter, this relation is as,

$$V_o = \frac{V_s N_2 D}{(1-D)N_1} \quad (3)$$

where D is the duty ratio of an isolated Cuk converter, which decides the turn on and off period of the switch.

In order to ensure DCM operation, the value of duty cycle D is considered to be 0.2, then the turns ratio of the HFT is calculated as,

$$\frac{N_1}{N_2} = \frac{V_{s\max} D}{(1-D)V_o} = \frac{198*0.2}{0.8*20} = 3.887 \quad (4)$$

Initially, when the switch S_1 is turned on, input voltage, V_S is applied to the input inductor, L_S resulting in linear increase in input current. Simultaneously, the intermediate capacitor, C_1 is discharged through switch S_1. On the secondary side of the high frequency transformer, the capacitor C_3 discharges its stored energy while diode D_1 remains reverse biased.

If the permissible ripple current flowing through the input inductor is Δi_{Ls} (30% of I_S), then the value of L_S is given as,

$$L_S = \frac{V_{s\max} D}{f_s \Delta i_{Ls}} = \frac{311*0.2}{50000*4.62} = 0.27\ mH \quad (5)$$

The selected value of input inductor is 0.32 mH to minimize the input current ripple.

When switch S_1 is turned off, the diode D_1 becomes forward biased. The input inductor, L_S discharges through intermediate capacitor, C_1 and the body diode of switch S_2. Furthermore, the output inductor, L_o delivers its stored energy to the welding load, R_o. Thus, the inductor current, i_{Lo} falls continuously and the rate of change in inductor current can be obtained from off period condition, which is as,

$$\frac{di_{Lo}}{dt} = \frac{-V_o}{L_o} \quad (6)$$

Thus value of output inductance at the boundary between CCM and DCM is given as,

$$L_{o\min} = \frac{V_o(1-D)^2 N_1^2}{2Df_s I_o N_2^2} = \frac{20*(0.8)^2(3.887)^2}{2*0.2*50000*120} = 80.58\ \mu H \quad (7)$$

Thus, the value of output inductor is estimated as L_{omin} = 80.58 μH.

To ensure DCM operation of an isolated Cuk converter,

$$L_o < L_{o\min} \quad (8)$$

Thus, the selected value of L_o is 26 μH. The output capacitor value can be calculated from eqn. (9) for a given voltage ripple (ΔV_o = 4% of V_o) as,

$$C_o = \frac{I_o}{4\pi f_L(\Delta V_o)} = \frac{120}{4*\pi*50*0.8} = 238.73\ mF \quad (9)$$

where f_L is the line frequency = 50 Hz.

The value of output capacitor is calculated as C_o = 238.73 mF to reduce the output voltage ripple.

Intermediate capacitance,

$$C = \frac{C_1 C_3 \left(\frac{N_2}{N_1}\right)^2}{C_1 + \left(\frac{N_2}{N_1}\right)^2 C_3} \quad (10)$$

The main function of the intermediate capacitor is to maintain nearly constant voltage within a switching period. The value of intermediate capacitance has a major impact on the input line current waveform. In order to minimise the input current oscillation, the resonant frequency of C, L_S and L_o' (referred value of L_o) should be greater than the line frequency.

Furthermore, the resonant frequency of C and L_o' must be less than the switching frequency to attain constant voltage during every switching cycle. Hence, the value of the capacitance can be approximated as,

$$C = \frac{1}{\omega_r^2 (L_s + L_o')} \quad (11)$$

$$= \frac{1}{5000^2 * \left\{0.32x10^{-3} + (26x10^{-6} * 3.887^2)\right\}}$$

$$= 56.12\ \mu F$$

where

$\omega_L < \omega_r < \omega_s$;

ω_L = line frequency, ω_r = resonant frequency and ω_s = switching frequency

Thus, the resonant frequency is selected to be 5000 Hz. For optimum operation, the calculated parameters are adhered to so that PFC feature of the proposed topology operating in DCM is maintained at different loads and AC mains voltages. These selected design parameters of the proposed converter system are summarized in Appendix.

IV. Performance Analysis of Proposed AWPS

In this section, the effectiveness of proposed bridgeless converter based AWPS is evaluated by simulating the proposed topology in MATLAB-Simulink environment. The converter circuit has been simulated for the calculated values of the bridgeless converter as given in Appendix to achieve unity power factor and low value of total harmonics distortion.

Figs 3-12 show the steady state and dynamic performances of the proposed converter. The converter operates in DCM to ensure improved power quality and high level of weld quality. The dynamic performance of the converter has been demonstrated by suddenly switching the welding load. The simulated results for light load and rated load conditions are shown in Figs. 3-7.

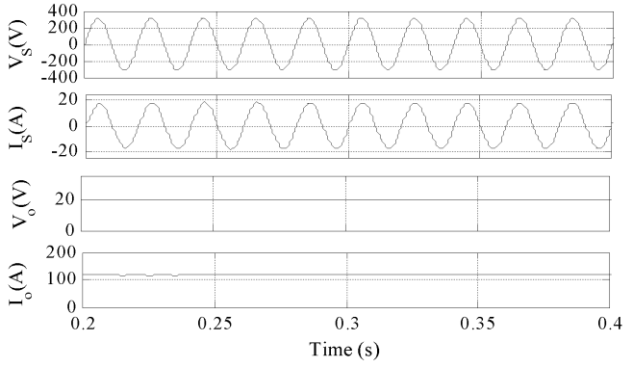


Fig. 3: Performance of proposed AWPS at 220 V AC mains and 100% load.

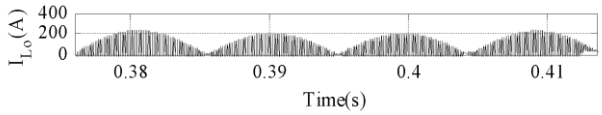


Fig. 4: Output inductor current of bridgeless Cuk converter demonstarting DCM.

In Fig. 4, it can be clearly seen that the converter is operating in DCM. The input and output voltage and current waveforms of proposed 2.4 kW welding power supply for a 20 V/120 A load is shown in Fig. 3. The input current waveform along with its harmonic spectrum and THD (Total Harmonic Distortion) of AC mains current for rated load condition are shown in Fig. 5. It is evident from Fig. 6 that even on varying loads, the system exhibits fast dynamic response. Moreover, the PI controller successfully maintains a constant DC voltage at output.

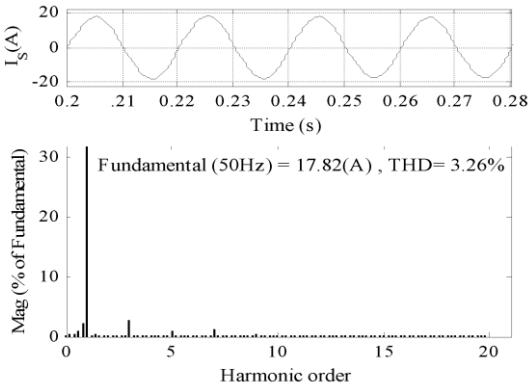


Fig. 5: Waveform and harmonics spectrum of AC mains current (I_S) at full load.

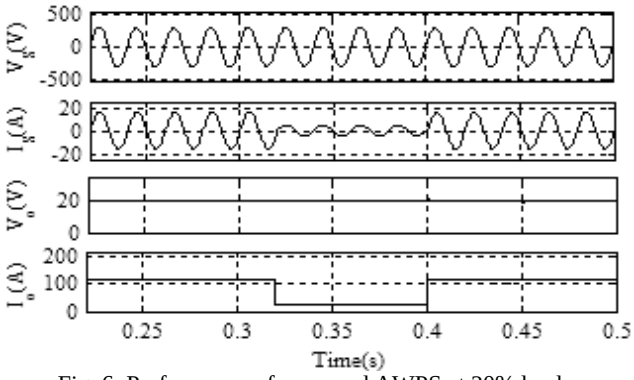


Fig. 6: Performance of proposed AWPS at 20% load.

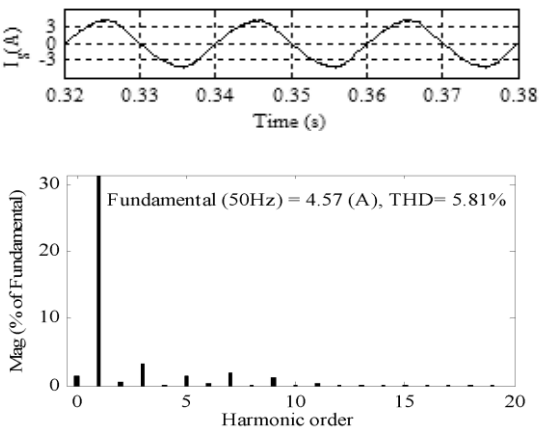


Fig. 7: Waveform and harmonics spectrum of AC mains current (I_S) at light load condition.

The harmonics spectrum of AC mains current along with its THD at light load condition is shown in Fig.7. The dynamic performance of welding power supply along with AC mains current frequency spectrum at varying supply conditions has been demonstrated in Figs. 8-11.

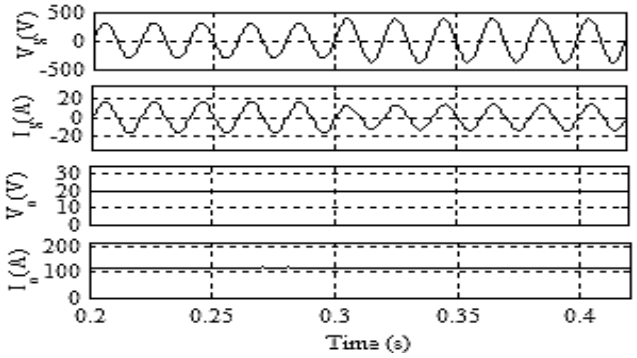


Fig. 8: Dynamic performance of the proposed AWPS at V_s of 270 V.

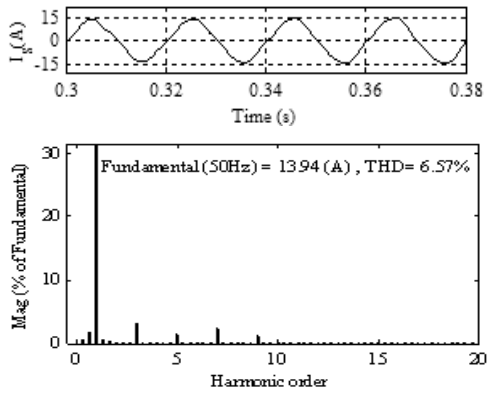


Fig. 9: Waveform and harmonic spectrum of AC mains current (I_S) at V_S of 270 V.

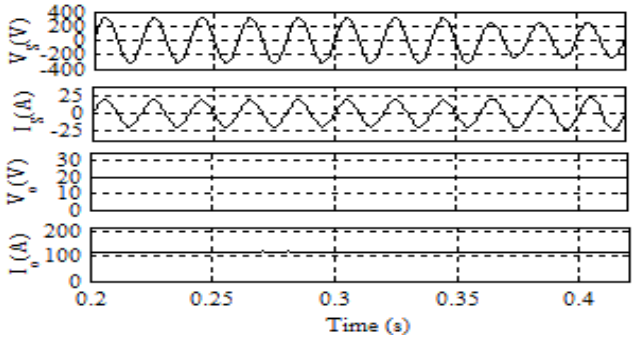


Fig. 10: Dynamic performance of the proposed AWPS at V_S of170 V.

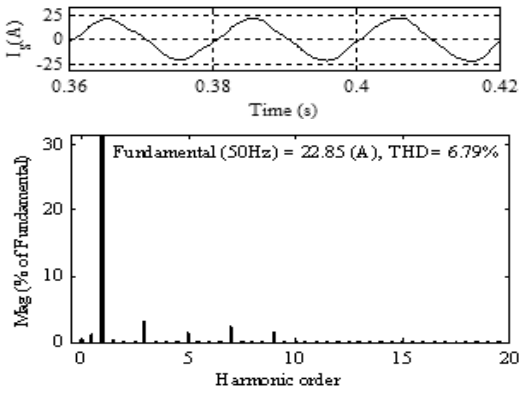


Fig. 11: Waveform and harmonic spectrum of input ac mains current (I_S) at supply voltage = 170 V.

The short circuit occurs when the electrode accidentally comes in contact with the welding pad and gets stuck to the molten metal. While designing an AWPS, it is beneficial to have a short circuit current slightly higher than the rated load current to inhibit the electrode from sticking to the work-piece during the arc striking process. Whenever the output current becomes more than 1.25 times the rated current, the PI current controller adjusts the duty cycle of the switches in such a way as to limit the output current to safe value.

The transition from short circuit to rated load condition is shown in Fig. 12. The controller aids in fast transition from short circuit to rated load and it restricts the output current to 150 A during short circuit period which results in less spatter generation and thus improves the weld quality.

Figs. 13-14 demonstrate the variation of PQ indices at various loads and input AC voltage variations. It can be clearly seen that the input AC mains current THD is below 5.81% under the variable load conditions while the input AC mains current THD is between 3.26% and 6.79% under the varying AC mains voltage.

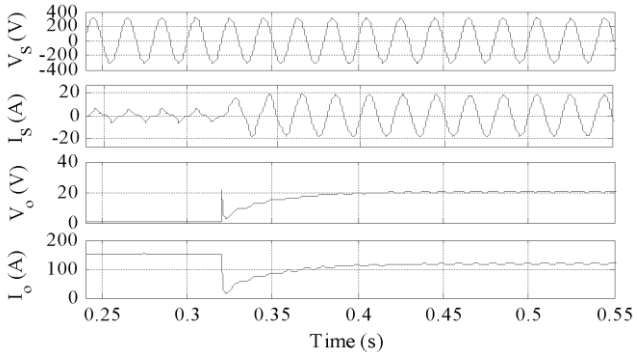
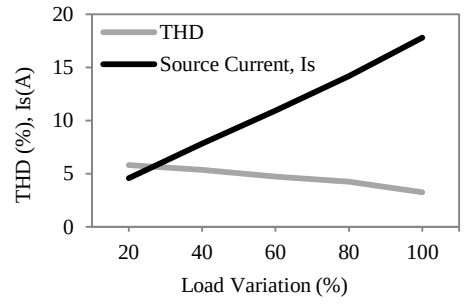
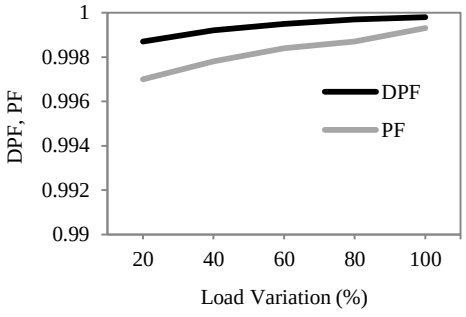


Fig. 12: Dynamic performance of proposed AWPS under short circuit condition.



(a)



(b)

Fig. 13: Variation of PQ indices of bridgeless Cuk converter based AWPS under different load conditions.
(a) I_S and its THD at AC mains
(b) DPF and PF

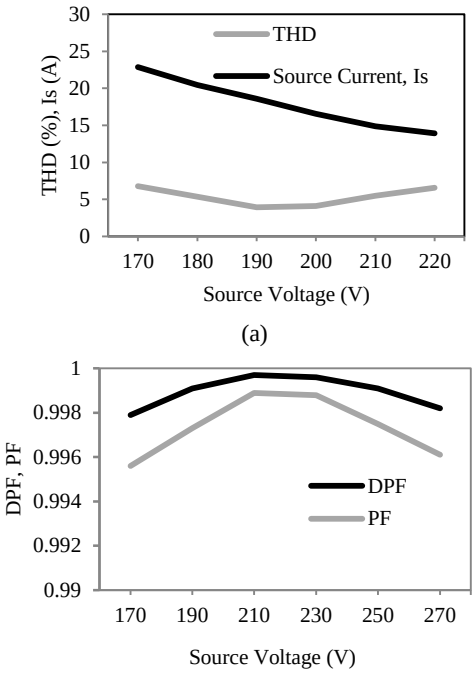


Fig. 14: Variation of PQ indices of bridgeless Cuk converter based AWPS under various source voltage conditions.
(a) I_S and its THD at AC mains
(b) DPF and PF

V. Conclusion

An exhaustive performance of a bridgeless Cuk converter based power supply for welding applications has been carried out for different loads and AC mains voltages conditions. It has been found that the THD of the input AC mains current falls within 7% for both full load as well as light load conditions for the wide range of operating AC mains voltage from 170V to 270V. Fast dynamic response of proposed welding power supply has been achieved hereby improving the reliability of the system. In addition, the proposed welding power supply has been found capable of operating even in the short circuit condition which makes the system more efficient and appropriate for welding applications. An effectual designing method to arc welding power supplies has been put forward.

VI. Appendix

Specifications of Proposed Welding Power Supply

Input AC mains voltage, V_s(rms): 220 V, 50Hz; Output Power, P_o: 2.4 kW; Output Voltage, V_o: 20V; Output Current, I_o: 120A; Switching frequency of DC-DC converter, f_S : 50 kHz; Transformer primary to secondary turns ratio, N_1/N_2: 3.887; Input Inductor, L_S = 0.32 mH; Intermediate Capacitor, C: 56.12 μF; Output Inductor, L_o: 26 μH; Output Capacitor, C_o: 238.73 mF.

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A Simple Transformerless Buck-Boost Switching Voltage Regulator

H. Prasad [1] T. Maity [2] V. K. Singh [3]

Abstract–This paper proposes a single phase ac-ac transformerless voltage regulator based on a simple ac-ac converter. The converter is analysed through state space averaging technique followed by small signal analysis. The proposed system employs a pulse width modulation (PWM) ac-ac converter along with feed-forward and PID closed loop control and uses power semiconductor device IGBT as bi-directional switch. This circuit can easily maintain constant voltage at the output to the end user and power quality problems both steady and dynamic in nature are arrested by this technique. The controller is designed based on its stability analysis. The system is verified with simulation and experimental results.

Keywords–Buck-boost, Pulse width modulation, PID, Sag, Surge, IGBT

I. INTRODUCTION

Traditional ac voltage regulators [1]-[3] are made with tap changer transformers. To obtain variable ac voltage from a constant ac voltage source, PWM single phase ac-ac choppers [4]-[6] have been widely used in ac power control applications such as light dimming, heater control, and ac motor speed control. There are different types of power quality problems exist in transmission and distribution system like transients, voltage sags, surges, harmonics and impulses. Because the power electronics technology has played a role in different areas in which technology can be manipulated into several forms. Again, the traditional single phase ac-ac converters are implemented by anti-parallel ac thyristor pairs or traic, employing phase angle or integral cycle control methods to obtain the desired output ac voltage. But, these techniques are having disadvantages like low power factor, high total harmonic distortion (THD) in the source current and poor power transfer efficiency. The proposed circuit is to design a transformerless voltage regulator having fast dynamic response and a good percentage of the voltage regulation. A single phase ac-ac voltage regulator is operating with a simple "feed-forward" design and PID closed loop control. The proposed circuit is to design a transformerless voltage regulator having fast dynamic response and a good percentage of the voltage regulation.

They have advantages like the better power factor, efficiency, and low harmonic contain in transmission line, easy control, smaller size and lower cost. It is a single stage ac-ac power conversion topology.

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Small Signal analysis is used to approximate the behaviour of nonlinear devices with linear equations. State space averaging is a powerful tool for analysis of pulse width modulated converters. Small signal analysis is used for the analysis of dynamic model of buck-boost circuit [7]-[10].

One of the main requirements is to study stability [11]-[15] of the system. In this paper, the stability analysis of the buck-boost converter in s domain is investigated by using the transfer function through different approach.

In this paper, the single phase ac-ac power converter is presented with a different kind of topology. The converter system is employing a feed-forward controller and PID controller which runs as an ac regulator under wide input variable condition. The high frequency switching of two set of bi-directional switch through proper duty ratio control can provide variable output voltage in buck-boost mode. Feed-forward control technique can eliminate the effect of the disturbance on the process output.

II. ANALYSIS OF THE CONVERTER

The topology of the buck-boost converter is a cascade connection of inductance and capacitance (Fig. 1). The main application of this circuit is in single phase ac chopper power supply, where a negative polarity output may be desired with respect to the common terminals of the input voltage. The output voltage can be controlled by changing the duty ratio. This output voltage may be higher or lower than input voltage, depending on the duty ratio. The circuit contains two bi-directional switches i.e. *S1* and *S2* with the inductor, capacitor and load. Switches *S1* and *S2* turn on alternately i.e. when S1 turns ON at that time *S2* turns OFF and vice versa. When S1 is closed and *S2* is open, source energy is dumped into inductor. That means source power does not transferred into load. When *S2* is closed and *S1* is open, the stored energy inductor is transfer through *L-S2-* load. If both switches are open, then no power is transferred to be source to the load. When duty ratio is less than 0.5, it operates in buck mode and when duty ratio is larger than 0.5, it operates in boost mode.

The relationship between input and output voltage is

$$Vo/Vi = -D/(1-D) \quad (1)$$

where V_o is the output voltage, V_i is the input voltage and D is duty ratio. The negative sign indicates the output phase is out of phase with the input. The open loop buck boost characteristic is shown in Fig. 2.

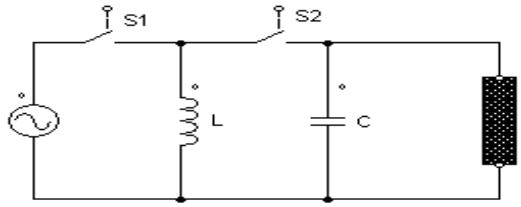


Fig. 1: Topology of the ac-ac converter

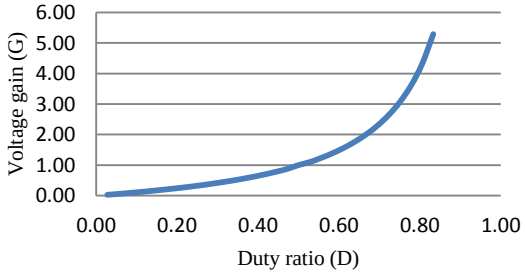


Fig. 2: Open loop characteristics of the converter

III. Small Signal Analysis

Small signal modeling is a common analysis which is used to approximate the behaviour of nonlinear devices with linear equations. Since most of the systems are non-linear in nature, hence we require linearization. The assumptions made for the purpose are: Inductors, capacitors, and resistors are linear, time invariant, and frequency independent, all semiconductor switches, i.e. the IGBT and diode are ideal switch. The converter time constant of the circuit is much larger than one switching time period.

Now, assuming input voltage - v_i, output voltage - v_o, voltage across inductors - v_L, voltage across capacitors - v_C, current through inductors - i_L , output current-i_o, and input current -i_i .

Also, order of the system = 2, states of the system- $X = \begin{bmatrix} i_L \\ v_C \end{bmatrix}$, inputs of the system- $u = \begin{bmatrix} v_i \\ i_o \end{bmatrix}$, output of the system- $y = \begin{bmatrix} v_o \\ i_i \end{bmatrix}$.

Now, when S1 is closed and S2 is open i.e. during [DT], where D and T are the duty cycle and time period respectively, the Fig. 3(a) gives the state equation as

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & -1/C \end{bmatrix} \begin{bmatrix} V_i \\ i_o \end{bmatrix} \quad (2)$$

When *S2* is closed and *S1* is open, i.e. during [(*1-D*) *T*], the state equation is derived as from Fig. 3(b)

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_C} \end{bmatrix} = \begin{bmatrix} 0 & 1/L \\ -1/C & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -1/C \end{bmatrix} \begin{bmatrix} V_i \\ i_o \end{bmatrix} \quad (3)$$

We take signals as a sum of steady state value and small signal value. In the other words, we apply perturbations to the quantities as follows-

$v_i = V_i + \hat{v_i}$, $i_i = I_i + \hat{i_i}$, $i_L = I_L + \hat{i_L}$, $v_C = V_C + \hat{v_C}$, $v_o = V_o + \hat{v_o}$, $i_o = I_o + \hat{i_o}$, $d = D + \hat{d}$ *where* $\hat{v_i}$, $\hat{i_i}$, $\hat{i_L}$, $\hat{v_C}$, $\hat{v_o}$, $\hat{i_o}$, $\hat{d}$ are small signal value and steady state value V_i, I_i, I_L ,V_C ,V_o I_o, D.

After application of perturbation, we apply state space averaging method to obtain the average model as

$$\hat{x} = \bar{A}.\hat{x} + \bar{B}.\hat{u} + [(A_1 - A_2).X + (B_1 - B_2).U].\hat{d} \quad (4)$$

where
$\bar{A} = A_1.D + A_2.(1 - D)$ and $\bar{B} = B_1.D + B_2.(1 - D)$

where, *A1* and *A2* are System matrix and *B1* and *B2* are input matrix.

Similarly, small signal output equation will be as follows-

$$\hat{y} = \bar{C}\hat{x} + \bar{D}.\hat{u} + [(C_1 - C_2).X + (D_1 - D_2).U].\hat{d} \quad (5)$$

Then, the state space averaging equation is derived as

$$\begin{bmatrix} \hat{i_L} \\ \hat{v_c} \end{bmatrix} = \begin{bmatrix} 0 & -(D-1)/L \\ (D-1)/L & 0 \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \hat{v_C} \end{bmatrix} + \begin{bmatrix} D/L & 0 & (v_i - v_C)/L \\ 0 & -1/C & i_L/C \end{bmatrix} \begin{bmatrix} \hat{v_i} \\ \hat{i_L} \\ \hat{d} \end{bmatrix} \quad (6)$$

The output equation is derived as

$$\begin{bmatrix} \hat{v_o} \\ \hat{i_i} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ D & 0 \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \hat{v_C} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & i_L \end{bmatrix} \begin{bmatrix} \hat{v_i} \\ \hat{i_o} \\ \hat{d} \end{bmatrix} \quad (7)$$

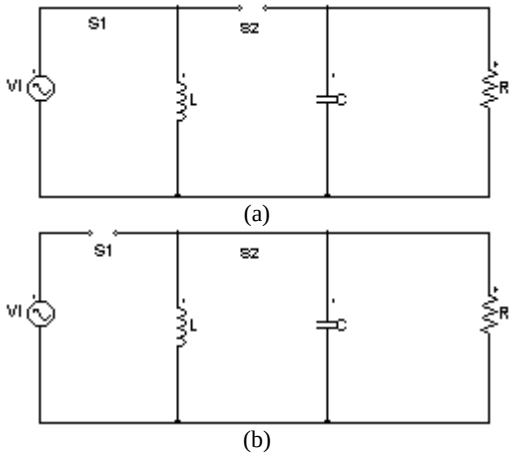


Fig. 3: Equivalent circuit (a) when *S1* is on and *S2* is off (b) when *S2* is on and *S1* is off

IV. Stability Analysis

Transfer function is derived for the converter considering its operating value D = 0.667, input Voltage = 200V, voltage across C = 400V, L = 0.8mH, C = 20 µF.

$$G(s) = \frac{2.5\times10^5 S + 3.918\times10^7}{S^2 + 6.523\times10^4} \quad (8)$$

It is clear from pole-zero map of the above transfer function that poles are located on imaginary axes. The pole location of the system in Fig. 4 shows that the system is marginally stable.

Now, the closed loop transfer function with unity feedback is given as-

$$G(s) = \frac{2.5\times10^5 S+3.918\times10^7}{S^2+2.5\times10^5 S+3.924\times10^7} \quad (9)$$

It is clear from unity feedback system pole-zero plot shown in Fig. 5 that poles are located in left half of the s-plane. The close loop transfer function goes on stable.

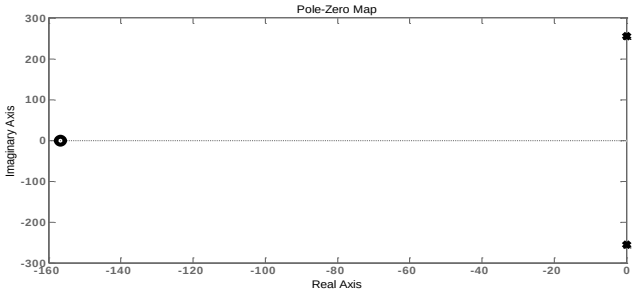


Fig. 4: Pole-zero map of open loop control system

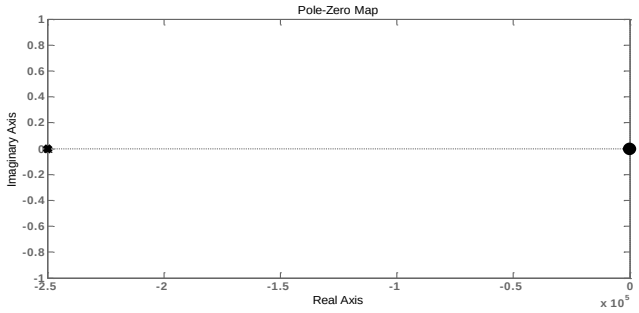


Fig. 5: Pole- zero Map of unity feedback system

V. PROPOSED VOLTAGE REGULATOR

As the closed loop system with unity feedback is stable system, it needs to design a controller which improves the stability of the previous systems and provide a stable output voltage. So, a PID controller is used to get the desired output, which includes various methods to get appropriate design parameters of the PID controller. This is further verified by direct tuning method and 'sisotool' in MATLAB. So the controller provided control transfer function with unity feedback is given by:

$$G_{CV}(S) = 0.1\frac{(1+2.4\,S)}{S} \quad (10)$$

After the application of controller, the poles of the system is shifted to left side of the s-plane and also the system looks highly stable by its step response as indicated in Fig. 6. The schematic diagram of the system is presented in Fig. 7.

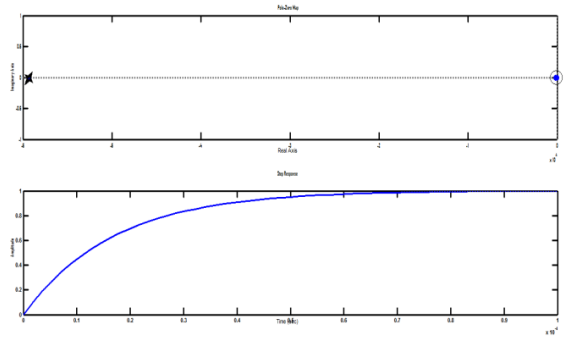


Fig. 6: Pole- zero Map and Step response of unity feedback system with controller provided

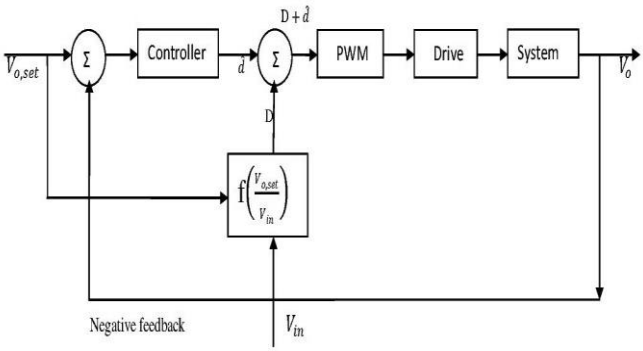


Fig. 7: Proposed closed loop system

VI. RESULTS AND DISCUSSION

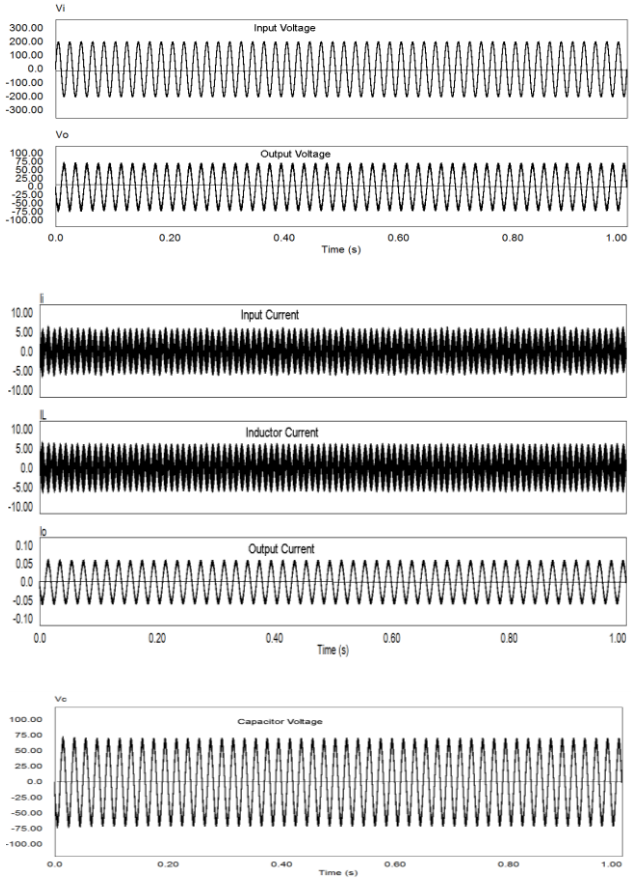
In order to verify the proposed single phase ac-ac converter in open loop, the PSIM simulation software is used. The components are chosen for simulation are L = 0.8mH, C = 20 μF, and Resistive load = 1200ohm. The bidirectional switches are designed with two IGBTs connected back to back in series. The switching frequency was set to 5 KHz and input sinusoidal voltage is selected as 200V peak. When D = 0.25, the input voltage is buck to 46 V_{rms} from 141 V_{rms} at the output and when D = 0.67, the output voltage is boosted to 283 V_{rms} from 141 V_{rms} input voltage. The buck and boost operation is clear from the waveform shown in Fig 8(a) and 8(b). The output voltage waveform is out of phase with the input voltage. Because of that, the voltage stress across switch is more equal to sum of the input and output peak voltages. The switching stress is therefore increased during boost condition.

The proposed single phase closed loop ac-ac regulator has the buck-boost capability i.e. it can operate in buck or boost mode depending upon desired output voltage and this overcome the problem of voltage sag or voltage surge in power system. Simulation result is carried out based on the proposed control system. The feed-forward system automatically selects the value of gain and accordingly the desired output voltage. A set of results shown in Table I prove its capability of buck, boost and regulation.

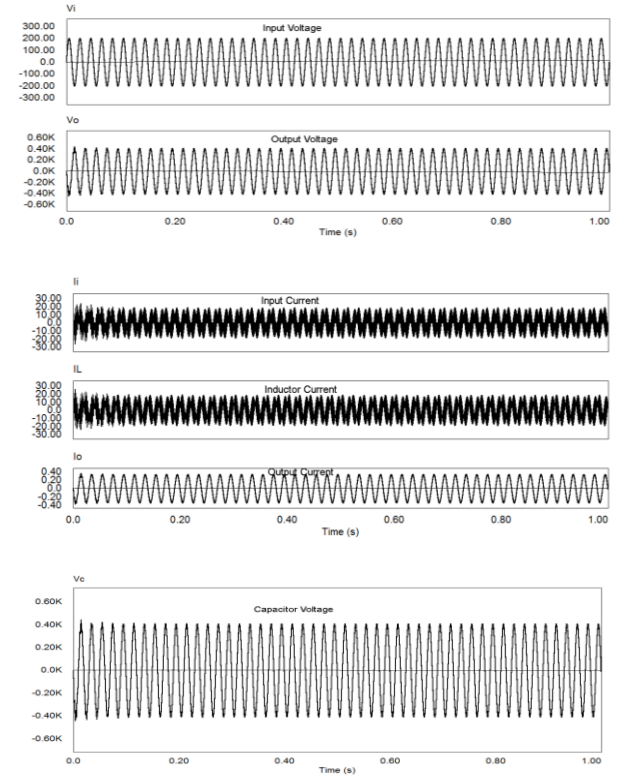
To check its dynamic response, input voltage is varied suddenly. First a voltage surge is applied at steady running condition from 170V to 280V rms and then voltage sag is applied over the steady voltage from 200V to 140V rms.

The input and output voltage waveforms are recorded in Fig. 9 and Fig. 10 respectively for sag and surge conditions and it shows a steady value except some small transient during change over instant in both the cases.

The laboratory based experimental setup is also done for analysis, the control is implemented with microcontroller and it will provide to voltage regulation as a viable solution. The experimental waveform of output voltage is shown in Fig. 11.



(a)



(b)

Fig. 8: Waveforms for Input voltage (V), Output voltage (V), Input current (A), Inductor current (A), Output current (A) and Capacitor voltage (V) under open loop condition of the converter at (a) Buck mode with *D*= 0.25 (b) Boost mode with *D*=0.67

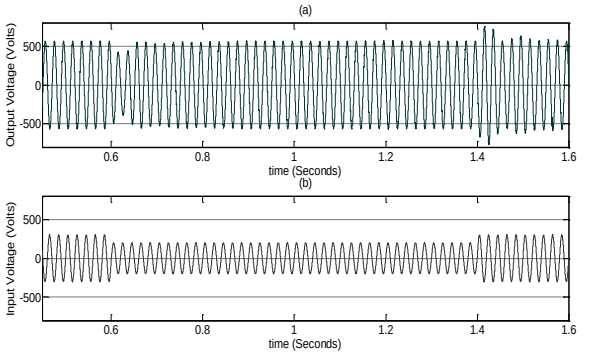


Fig. 9: Waveforms with PID Controller during input voltage Sag condition .(a) Output Voltage. (b) Input Voltage.

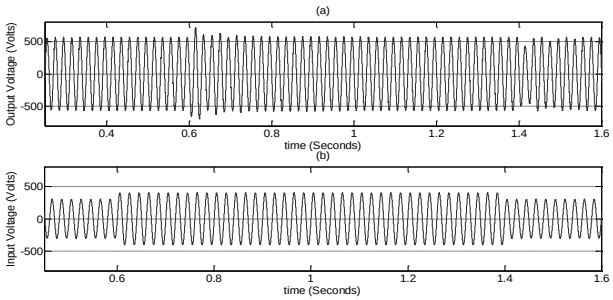


Fig. 10: Waveforms with PID Controller during input voltage Surge condition .(a) Output Voltage. (b) Input Voltage.

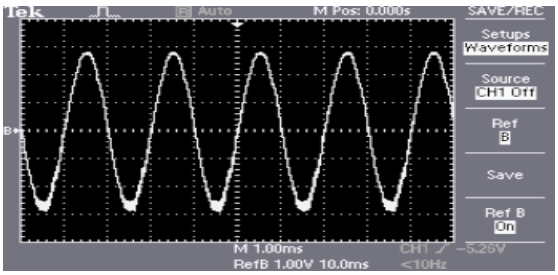


Fig. 11: Experimental waveform of output voltage

Table 1: Simulation and experimental results showing buck-boost and regulation (Output set value = 200V)

Input Voltage (Vrms)	Simulation Output Voltage (Vrms)	Experimental Output Voltage (Vrms)
230V	210.60V	205.60V
220V	210.0V	203.50V
200V	208.10V	203.0V
184V	207.20V	200.80V
170V	200.30V	197.60V
163V	199.20V	196.0V
150V	198.75V	194.80V

VII. CONCLUSION

In this paper, a novel simple single phase ac-ac buck-boost converter with closed loop feed-forward control and PID control are proposed. With a simple technique single phase AC-AC converter can keep the output voltage steady by operating at buck-boost mode. The proposed topology has the capability to overcome the voltage sag or voltage surge

in transmission line and distributed power system. This work shows that ac-ac converter performs well during the voltage fluctuation. The operating principle, steady-state and transient analysis of the system were presented. To verify the proposed system, the simulation and laboratory based experiments are carried out. The fast response will allow rural power consumers, to better withstand variable voltage conditions and can provide reliable and quality power supply. The proposed circuit is simple, robust and low cost. It has only drawbacks like inverted phase at the output and maximum voltage stress across switches.

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Impact of Variable Hysteresis Control in Evaluating the Performance of an Ultra-Capacitor Configured Energy Storage System for Electric Vehicles

Shrikant Misal [1] B.P. Divakar [2]

Abstract– Uncontrolled frequent charging and discharging of batteries is of great concern to Electric Vehicle manufacturers. The idea wherein the battery is made to supply a constant base load with an energy buffer taking care of transient load is gaining acceptance. Ultra-capacitor can undergo several charge-discharge cycles and absorb/deliver energy for short durations such as during acceleration and deceleration. Because of this property, hybrid energy storage system concepts have been developed by interfacing ultra-capacitors and batteries. There are many ways in which the hybrid energy storage system can be configured in electric vehicles. In this study, a topology wherein, the ultra-capacitor is interfaced with the battery through a bi-directional converter is considered and analyzed. The performance of the hybrid system in which the capacitor voltage is controlled with hysteresis control is studied in detail and several limitations with the control have been brought out. Results reveal that there is a need for adjusting the hysteresis window, so as to control the power being delivered from or to the battery. The study aids sizing of capacitor in the hybrid system.

Keywords– Electric vehicle (EV), battery, ultra-capacitor (UC), hybrid energy storage system (HESS), bidirectional DC-DC converter, hysteresis window

I. INTRODUCTION

Energy Storage System (ESS) is one of the most important components of an electric vehicle that play a vital role in improvising the overall performance of the complete drivetrain configuration. A conventional battery-based ESS possess several limitations which are needed to be worked upon like: i) Low power density ii) Thermal Management iii) Cell Balancing iv) Frequent charge-discharge cycles leading to deterioration v) Size and cost. In a typical urban driving condition, owing to sudden acceleration and braking actions of an Electric Vehicle (EV), batteries are subjected to transient loads very often. Research works have already proved that the batteries when subjected to a constant load profile perform more efficiently and can last longer. Hence to overcome these limitations of a conventional battery based energy system as highlighted above, different Hybrid Energy Storage System (HESS) configurations integrating battery and ultra-capacitor (energy buffer) have been suggested in literatures [1-4], [6] and [7]. Interfacing the battery and an ultra-capacitor through a controlled dc/dc converter results in battery size reduction and better overall performance [1], [3] and [6].

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There are few configurations for HESS design proposed in literatures [1-8] and [10-12] wherein battery and ultra-capacitor are configured uniquely to share the load. Some of the prominent configurations are i) Ultra-capacitor/Battery configuration having UC at the input of dc/dc converter and Battery at its output. The advantages associated with this configuration are: a) The battery which is directly connected to the DC link yields a rather constant DC link voltage and b) The UC energy can be used in a wide range by controlling bi-directional dc/dc converter. The disadvantages associated with this configuration are: a) there is no means to protect the battery from transients and b) the bi-directional converter should be rated to handle the UC power in addition to the load demand. ii) Battery/Ultra-capacitor configuration having battery at the input and ultra-capacitor at the output of dc/dc converter. The advantages associated with this configuration are: a) requires battery with lower voltage rating b) better utilization of the energy stored in UC because the UC voltage is allowed to swing in a wide range. The only limitation associated is that the design calls for optimization of UC and converter size for better utilization of energy. iii) Cascaded configuration implements two dc/dc converters in cascade in such a manner that second converter is connected at the output of first. This is an extended version of Battery/UC configuration. A major advantage associated with this configuration is that UC voltage can be further controlled in much more efficient and precise manner to meet the variable load requirements. The only disadvantage associated with this configuration is the overall cost since two converters are implemented. iv) Multiple Input Converter configuration permits series connection of converters for high voltage application. The advantages associated with this configuration are: a) High voltage implications of dc link can be efficiently met since both the energy buffers are not unduly stressed and b) The UC energy is fully utilised resulting in battery size reduction. Few disadvantages associated with this configuration are the complexity of the system as well as the challenge of optimizing the sizes of both battery and UC to meet the requisite power demands. v) Multiple Converter configurations paralleling the output of two converters instead of cascading [1]. The advantages associated with this configuration are the use of two dc/dc converters with input from energy buffers helps in effective optimization of energy associated with each buffer resulting in reduced stress on the battery. The disadvantages associated with this configuration are increased cost and complexity.

The configuration, in which a bidirectional converter is interfaced between a battery and an ultra-capacitor, is the widely preferred topology [12-15]. Even though this design alleviates the peak power seen by the battery, the battery is still subjected to frequent charge and discharge

operations. A Battery/Ultra-capacitor configuration is implemented in [1] where the ultra-capacitor is directly connected across the load so as to meet the power demanded by the load. This configuration has the advantage of flexibility in varying the dc link voltage in accordance with frequent charge and discharge operations of the ultra-capacitor.

Organization of the paper

The HESS configuration presented in [1] is introduced in II, significance of hysteresis window in III, mathematical modeling of the bidirectional converter in IV, simulation of mathematical model in V and various simulation studies in VI, inferences drawn from simulations in VII followed by concluding remarks in VIII.

II. Ultra-Capacitor Configuration

A. *Operation Of Battery/Ultra-Capacitor HESS Configuration :*

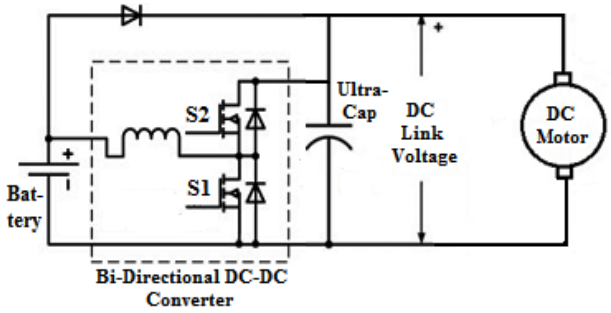

Fig.1: Battery/Ultra-Capacitor Configuration [1]

An ultra-capacitor based energy storage system configuration is as shown in Fig.1 wherein the battery is interfaced with the ultra-capacitor through a bidirectional dc-dc converter that acts as a boost converter in the forward mode and buck converter in the regenerative mode.

The function of the capacitor is to transfer and absorb transient energy thereby making the battery see a stable load. Thus it protects the battery against frequent charge/discharge cycles thereby extending the life of the battery. Since the battery voltage is stepped by boost action, this configuration requires less number of batteries in the string.

B. *Control Strategy :*

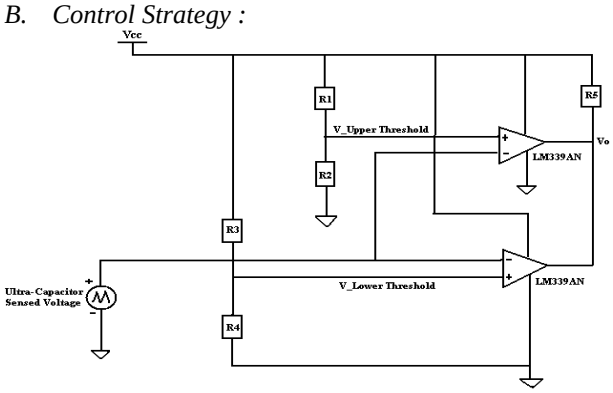

Fig.2 Circuit Diagram of Window Comparator

The capacitor is expected to deliver or absorb energy as and when required by the load so that the battery supplies a steady load. As the energy supplied or absorbed depends on the difference of the square of the maximum and minimum voltage of the capacitor, the voltage swing of the capacitor has to be monitored and controlled for effective operation of the system. In present scheme, the well-known hysteresis method, in which the capacitor voltage is maintained within an upper and lower limit, has been employed. The band width plays a significant role during forward and regenerative mode of the bidirectional converter. Hence the main focus of this paper is to present various options for choosing hysteresis band and their effectiveness in satisfying the energy requirements. Fig.2. shows the schematic of the window comparator wherein two op-amps compare the capacitor voltage with upper and lower reference value respectively.

C. *Generation of PWM Signals for Lower and Upper Switch:*

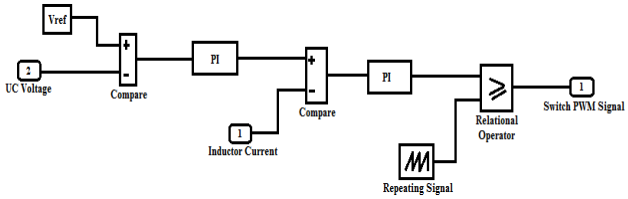

Fig.3 Block diagram of PWM Sub-system

The operating mode of the motor load: forward or regenerative, influences the switching action of the dc-dc converter. The gate signal generation scheme is incorporated using a PWM subsystem as shown in Fig.3 above. Here current mode control has been employed for controlling the battery current during forward and regenerative modes.

The current in the inductor is sensed and compared with a reference signal which is produced from the PI controller to which the error between the sensed capacitor voltage and the reference is fed. The error between the sensed inductor current and the commanded value is again passed through the second PI controller and compared with the ramp signal for controlling the switches. Through the pulse steering circuit, the generated signals are applied to the appropriate switches depending on the mode of converter operation.

III. Significance Of Hysteresis Window

The energy stored in an ultra-capacitor is a function of the magnitude of capacitance value and the square of the hysteresis band/window as shown in Eq. (1).

$$E_{UC} = (1/2)\, C\, (V^2_{max} - V^2_{min}) \qquad (1)$$

where

E_{UC} = Energy stored by ultra-capacitor

V_{max} = Upper threshold voltage level attained by capacitor

V_{min} = Lower threshold voltage level attained by capacitor

And $$E_{UC} = P_O\, T_D \qquad (2)$$

$$E_{UC} = P_{IN}\, T_C \qquad (3)$$

where,

P_O = Output power delivered by the ultra-capacitor
P_{IN} = Input power absorbed by the ultra-capacitor
T_D = Discharge time of ultra-capacitor
T_C = Charging time of ultra-capacitor

From Eq. (1) one can observe that the energy stored and released by the capacitor depends on the two thresholds. Similarly from equations (2) and (3) one can observe that the power delivered or absorbed by the capacitor varies inversely with the respective discharging or charging period of capacitor. Hence it can be concluded that the energy stored or released by the ultra-capacitor can be controlled by controlling the hysteresis band or the charge/discharge period.

IV. Mathematical Modeling Equations Of Bi-Directional Converter

Mathematical model of the bi-directional converter for both boost and buck mode of operation can be realised based on the operation of motor load connected at its output i.e. boost operation for motoring mode and buck operation for regenerative mode. The equations governing this bi-directional operation of the converter are:

Buck Mode:

$$(di_L/dt) = [V_g - (1-D)V_o] / L \quad (4)$$

$$(dV_o/dt) = [\, i_L - i_o \,] / C \quad (5)$$

Boost Mode:

$$(di_L/dt) = [(1-D)V_o - V_g] / L \quad (6)$$

$$(dV_o/dt) = [\, i_o - i_L \,] / C \quad (7)$$

where,

i_L = Current through Inductor
i_o = Converter Output Current
V_g = Input Voltage of Converter
V_o = Output Voltage of Converter

Since the inductor current (i_L) and the output voltage (V_o) of the converter are responsible for determining its overall performance hence equations (4) to (6) have a significant role in developing a mathematical model for implementing the simultaneous boost and buck operation of the converter. Eq. (4) governs the boost operation of the converter with a duty cycle '*D*' while Eq. (6) governs the buck operation of the converter.

V. Simulation of Mathematical Model For Converter Circuit

The Fig.4 below shows a complete mathematical model of the bi-directional converter depicting the cyclic forward and regenerative operation of the motor load.

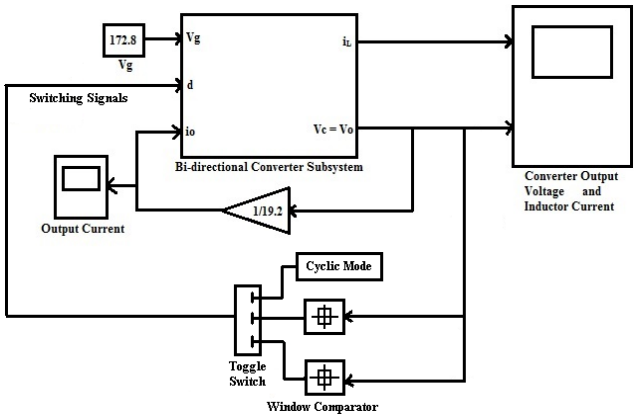

Fig.4: Bi-Directional Converter Mathematical Model

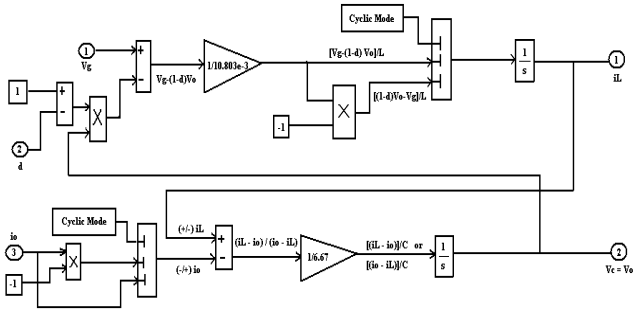

Fig.5: Bi-Directional Converter Sub-system

Fig.5 represents the bi-directional converter sub-system realizing equations (4) to (7) for its respective boost and buck operation as discussed in the previous section. The model has been developed to depict the bidirectional features of the system simultaneously.

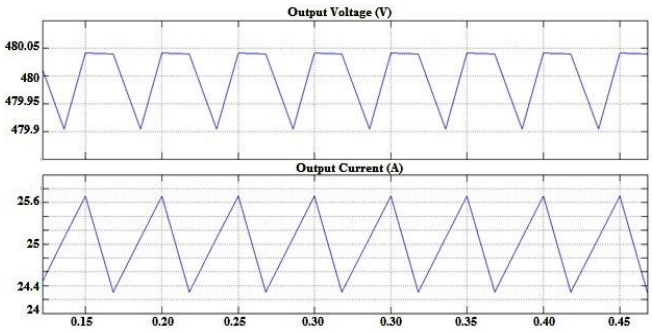

Fig.6: Simulation Results in Boost Mode. Top: Capacitor Output Voltage and Bottom: Output Current

The simulation results from the model shown in Fig.4 are shown in Figures 6 and 7 for the forward mode (generation mode or boost mode) and regenerative mode (buck mode) respectively. During forward mode, the output voltage is tightly regulated at 480V for an input voltage of 172.8V from the battery. The capacitor voltage almost remains constant at 480V because of the 0.15V hysteresis window. The inductor current of the boost converter has an average value of 25A with a ripple content of 1.4A. The on period is indicated by the up-slope of the inductor current while the off period is indicated by the down-slope of the inductor current. The capacitor discharges during the on time and support the load till the switch is turned off. During the off period, the energy stored in the inductor is used to charge the capacitor and to supply the load.

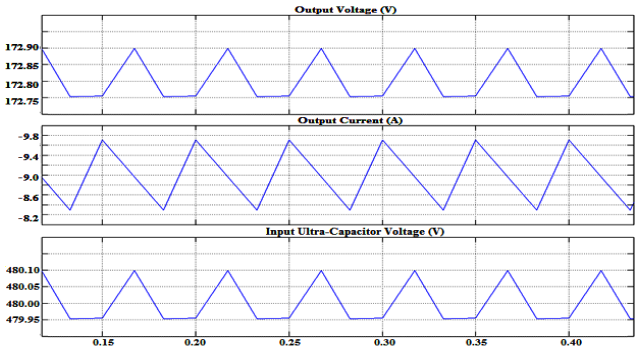

Fig.7: Simulation Results in Buck Mode. Top: Rated Battery Voltage. Middle: Battery Charging Current and Bottom: Input Capacitor Voltage

The bidirectional model can also describe the operation during regeneration in which the capacitor is made as the source and battery as the sink. In the regenerative mode, the load current is reversed and the capacitor is made as the source feeding the bidirectional converter which now is operated in the buck mode.

In the regenerative mode, the capacitor's voltage as before is controlled within a hysteresis band of 0.15V. The plots shown in Fig.6 confirm the bidirectional capability of the mathematical model.

VI. HESS Circuit And Simulation Results

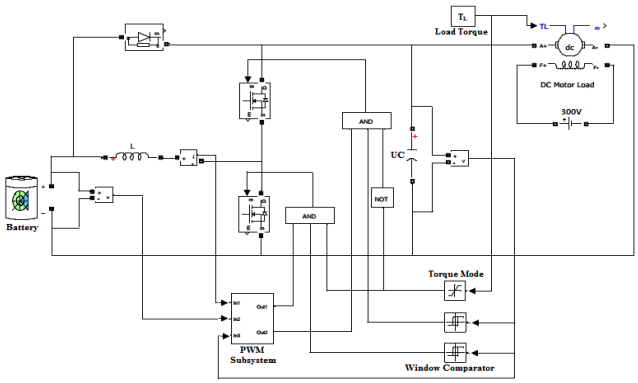

Fig.8: Complete Simulation Circuit of a Battery/Ultra-Capacitor HESS Configuration

The complete simulation model at the circuit level is depicted in Fig.8 and the simulation specifications are shown in Table I. As mentioned earlier, control of capacitor voltage influences the system's performance; hence several strategies highlighting their pros and cons are considered and discussed below.

Case I: Normal Window of Hysteresis

a) Forward Operation: With a Band (450 – 480)V for Load Torque (T_L) = 150Nm

In this mode of operation the capacitor voltage is allowed to vary between 450V and 480V. The characteristic of this mode is that the load is being supplied mainly by the battery and partly by capacitor as indicated by its discharge profile. The energy lost by the capacitor will be replenished by the battery in every cycle.

Table 1: Typical Ratings and Characteristics of the Components Used in Simulation

	Ni-Mh Battery	Ultra-Capacitor	DC-DC Converter	DC Motor Load
Specifications Used	172.8V, 180Ah	6.67F, 500V_{max}	Constant Efficiency, 12kW Continuous	100HP Max., 500V, 1750rpm
Nominal Cell Voltage (V)	1.25	2.5-2.7		Armature Parameters: R_a = 0.1968 Ω L_a = 0.00342H
Energy Density (Wh/Kg)	60-120	5-30		
Power Density (W/Kg)	220	4000-10000		Field Parameters: R_f = 58.82 Ω L_f = 7.267H
Charge/Discharge Cycles	300-500	Upto 1000000		
Operating Temperature (°C)	-20 to 65	-40 to 65		

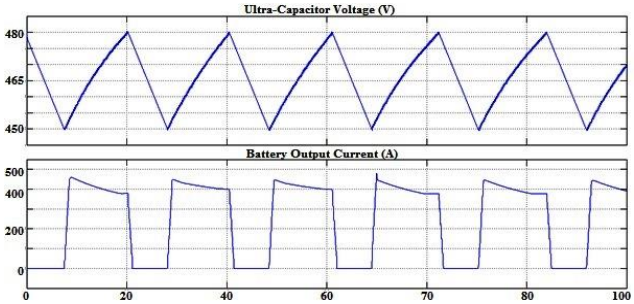

Fig.9: Simulation Results in Forward Mode for Normal Window. Top: Ultra-Capacitor Voltage and Bottom: Battery Current

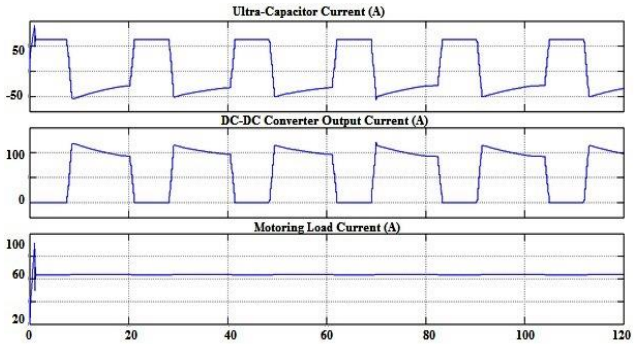

Fig.10: Simulation Results in Forward Mode for Normal Window. From Top: Ultra-Capacitor Current, DC-DC Converter Output Current and Motoring Load Current

Various plots are given in Figures 9 and 10 from which one can determine ratings of various devices. A 150 N-m of motor load will demand a peak current of 400A from the battery and that will translate into 100A peak of output current from bi-directional converter.

Hence the conducting switches S_1 and D_2 will see a peak current of 400A in the forward mode of operation. Because of the nature of the hysteresis band, the capacitor is allowed to discharge thereby the entire load of 63A is met by the capacitor alone. Thus the battery does not contribute during the time when the capacitor is able to meet the load demand on its own. As can be seen, the battery current is a series of high pulses which will reduce the life of the battery. Therefore, it can be inferred that the capacitor voltage should be properly regulated by dynamically adjusting the width of the window thereby allowing the battery to supply a constant base load.

b) Reverse Operation: With a Band (480 – 500)V for Load Torque (T_L) = -150 Nm

This case study pertains to the regenerative mode in which the regenerative load of 150Nm is considered and a

hysteresis band of (480-500)V is taken. The upper limit has been increased to 500V with an intention of storing higher energy in the capacitor, which can be utilized when the demand arises.

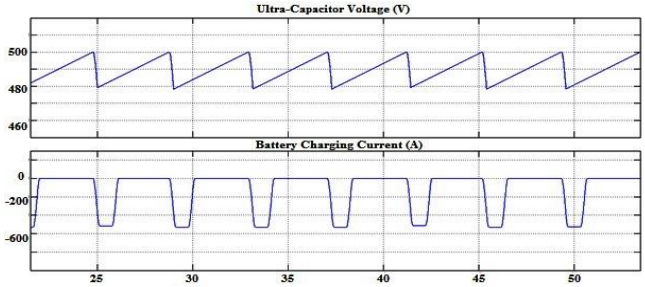

Fig.11: Simulation Results in Regenerative Mode for Normal Window. Top: Ultra-Capacitor Voltage and Bottom: Battery Current

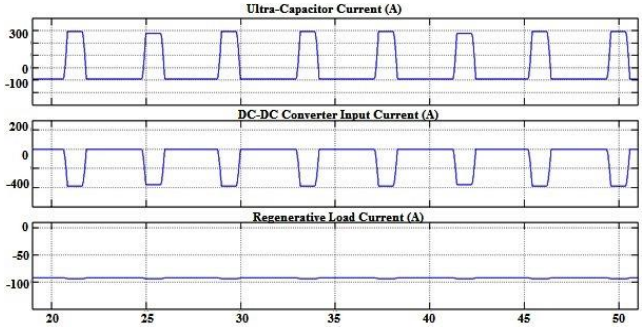

Fig.12: Simulation Results in Regenerative Mode for Normal Window. From Top: Ultra-Capacitor Current, DC-DC Converter Input Current and Regenerative Load Current

In the forward mode, 90A of regenerative current and 300 A peak from the capacitor are translated into 390A peak current at the input of the bidirectional converter. Hence the battery will be charged with a peak current of 530A due to buck operation. In this mode, switch S_2 and diode D_1 will be in conduction.

The capacitor is mainly responsible for absorbing the sudden inrush of regenerative power from the load and once it reaches the upper threshold of 500V, it discharges until the lower limit of 480V before the start of the next cycle. The simulation highlights hidden aspect of the window comparator. It helps the capacitor to store and discharge as much energy as desired depending on the hysteresis width. However, it will result in high discharge current from the capacitor during regeneration if measure is not taken to prevent unnecessary discharge by the capacitor.

c) Combined Forward and Reverse (Cyclic) Operation: For Load Torque (T_L) = 150 Nm and -100Nm

In this case the simulation is carried out with alternate forward and regenerate mode cyclically to test the validity of the model. Accordingly the cyclic mode of operation has been implemented for a fixed hysteresis voltage window of (450-480)V during forward torque and (480-500)V during regenerative mode. Here both the upper and lower limits are changed according to the mode of operation for effective utilization of capacitor energy. The switching signals for switches S_1 and S_2 are generated as per the mode of operation with the help of the mode detection block.

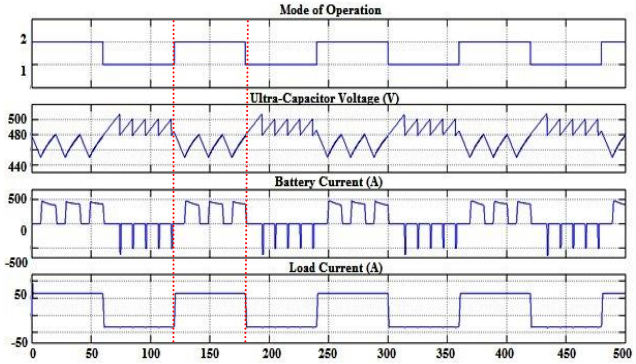

Fig.13: Simulation Results in Cyclic Mode From Top: Mode Signal, Ultra-Capacitor Voltage, Battery Current and Load Current

The simulation results for cyclic operation are shown in Fig. 13. The mode of operation is detected by the direction of the load current shown by the bottom trace. The positive polarity shows the forward mode while the negative polarity indicates the regenerative mode. In the forward mode, both the upper and lower limits of the hysteresis band are lowered to allow the capacitor to meet the sudden demand. Thus at the start of forward mode, the capacitor discharges until it reaches the lower limit from there it begins to charge from the battery towards the upper limit. Therefore from the start of the forward mode up to the point of lower limit, the battery remains idle. Similarly when the mode changes from forward to regeneration as indicated by the second vertical line, the upper and lower hysteresis windows are increased so as to permit charging of the capacitor thereby protecting the battery from sudden inrush power.

Case II: Increased Window of Hysteresis

a) Forward Operation: Hysteresis Window of (400 – 480) V for Load Torque (T_L) = 150Nm

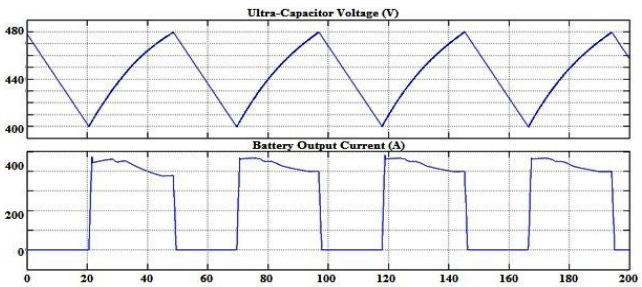

Fig.14: Simulation Results in Forward Mode for Increased Window. Top: Ultra-Capacitor Voltage and Bottom: Battery Current

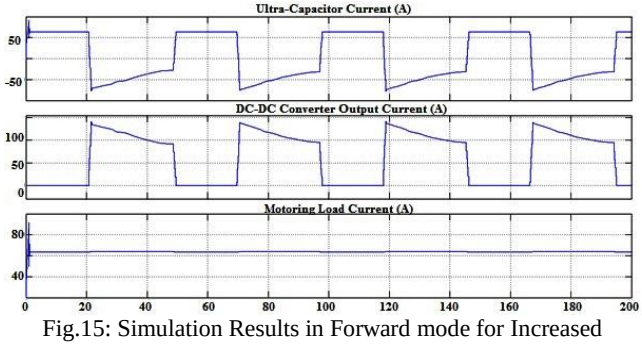

Fig.15: Simulation Results in Forward mode for Increased Window. From Top: Ultra-Capacitor Current, DC-DC Converter Output Current and Motoring Load Current

The simulations are carried out with an increased window of (400–480)V. This increased window has naturally increased the time taken to discharge the capacitor and has increased the energy stored by 1.52 times as compared to Case I. This increased energy will mitigate the sudden change in future power requirements.

b) Reverse Operation: Hysteresis Window of (450 – 500) V for Load Torque (T_L) = -150Nm

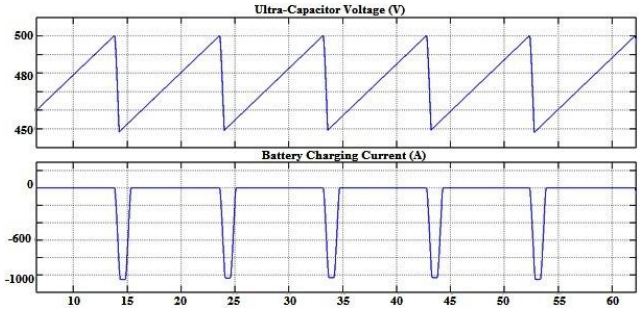

Fig.16: Simulation Results in Regenerative Mode for Increased Window. Top: Ultra-Capacitor Voltage and Bottom: Battery Current

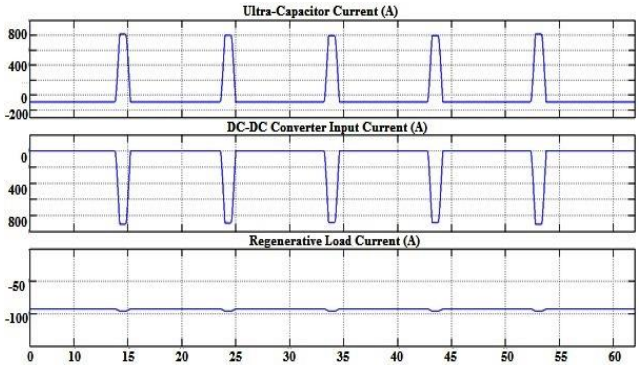

Fig.17: Simulation Results in Regenerative Mode for Increased Window. From Top: Ultra-Capacitor Current, DC-DC Converter Input Current and Regenerative Load Current

This case is similar to case I but with higher hysteresis window. The increased window permits storage of more regenerative energy in the capacitor thereby protecting the battery against inrush power.

c) Combined Forward and Reverse Operation: for Load Torque (T_L) = 150 Nm and -150Nm

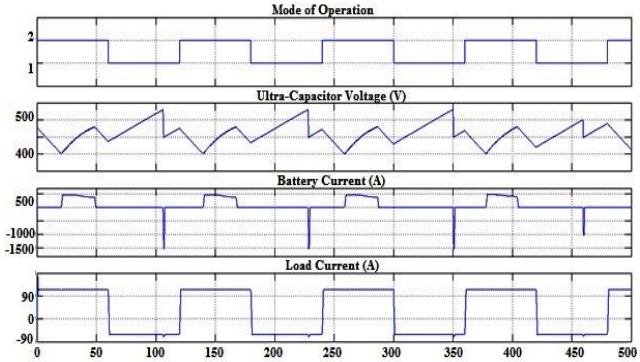

Fig.18: Simulation Results in Cyclic Mode from Top: Mode Signal, Ultra-Capacitor Voltage, Battery Current and Load Current

A simulation of combined forward and regenerative mode of operation is carried out as seen in Fig.18. During forward operation the upper limit is fixed at 480V while the lower limit has been decreased to 400V. The basic intention behind increasing the window is to make the UC discharge deeper so as to meet the load requirements for longer duration of time. Similarly for the regenerative operation the lower limit is fixed at 450V while the upper limit has been changed to 500V with intent to make UC store more regenerative power compared to Case I.

Case III: For Reduced Hysteresis Window Control

Simulation studies pertaining to the first two cases have brought out one basic drawback with the present control strategy that hysteresis window not only causes frequent charging-discharging of the ultra-capacitor but also of the battery. Because the capacitor is connected across the load and supplied by the battery, discharge of the capacitor can cause the battery to replenish the lost charge. If hysteresis control is employed with a large window, the battery will see a pulse load required to charge the capacitor.

Thus there is a serious limitation associated with this topology wherein the capacitor is directly connected across the load and made to meet the change in load demand. Taking account of above situation, the desirable option would be to maintain a steady voltage across the capacitor for constant power loading which can cause the power delivered from the battery to be constant for constant load thereby extending the battery life.

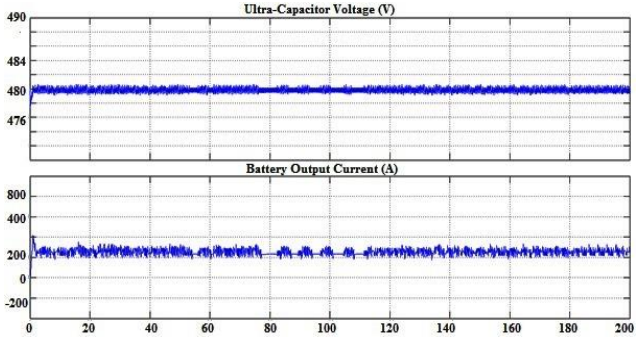

Fig.19: Simulation Results in Forward mode for Reduced Window Top: Ultra-Capacitor Voltage and Bottom: Battery Current

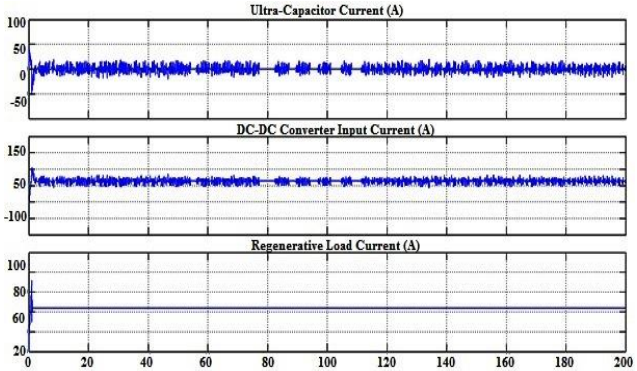

Fig.20: Simulation Results in Forward mode for Reduced Window from Top: Ultra-Capacitor Current, DC-DC Converter Output Current and Motoring Load Current

So considering these aspects, a case study with a very small window of Hysteresis i.e. (480-479.8) V for the forward operation and (499.8-500)V for the reverse operation of the motor load has been carried out. During forward operation as shown in Figures 19 and 20,

an average battery input of 225A will be responsible for charging the capacitor at a constant current of 63.75A through Boost operation of converter. Similarly for regenerative operation shown in Fig. 21 and 22, a constant regenerative current input of 93A will be charging the battery at a constant current of 200A through buck operation.

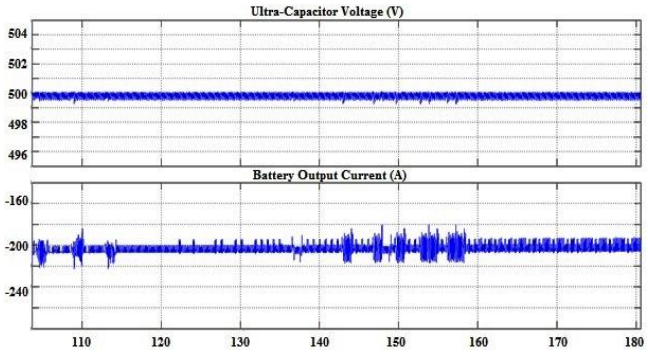

Fig.21: Simulation Results in Regenerative Mode for Reduced Window. Top: Ultra-Capacitor Voltage and Bottom: Battery Current

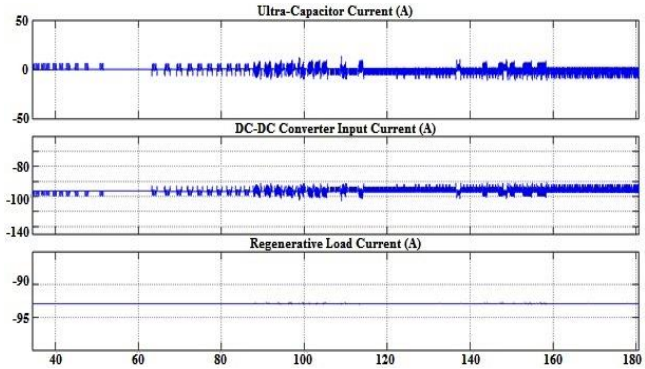

Fig.22: Simulation Results in Regenerative Mode for Reduced Window. From Top: Ultra-Capacitor Current, DC-DC Converter Input Current and Regenerative Load Current

With the reduced window, the capacitor voltage has been confined within a smaller band resulting in tighter control over charging and discharging of the capacitor. From the view point of longevity of capacitor this profile is very much favorable but it will not permit the capacitor to either discharge during sudden change in the load as happens during acceleration of motor load or to charge during regeneration.

Case I, II and III considered simulation under various windows and highlighted their advantages and limitations. For cases I and II, the battery is subjected to pulse currents of high magnitude. On the other hand the simulation with reduced window as in case III overcomes the above limitation but it does not allow the capacitor to share the load during forward and regenerative modes. So the desirable feature is to have the windows dynamically changed with respect to the mode of operation as well as the load thereby letting the capacitor to participate actively in load sharing with the battery.

A simulation study is therefore carried out with dynamically changing windows during forward and regenerative modes. In this study, four cycles lasting for 125 sec are considered. The first two cycles are for the forward operation with increased and reduced windows respectively. The next two cycles are for the regenerative mode with increased and reduced windows respectively. The results are depicted in Figures 23 and 24.

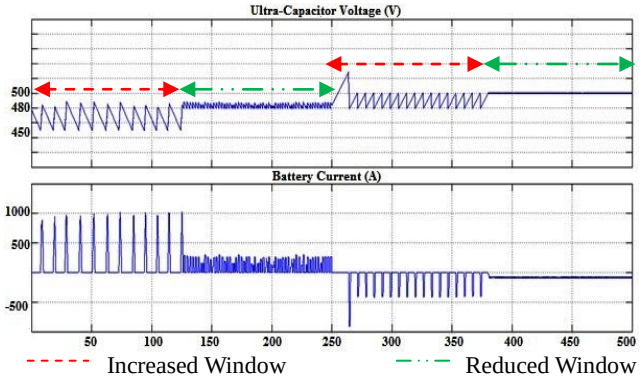

Fig. 23: Simulation Results for Combined Mode with Variable Window; Top: Ultra-Capacitor Voltage and Bottom: Battery Current

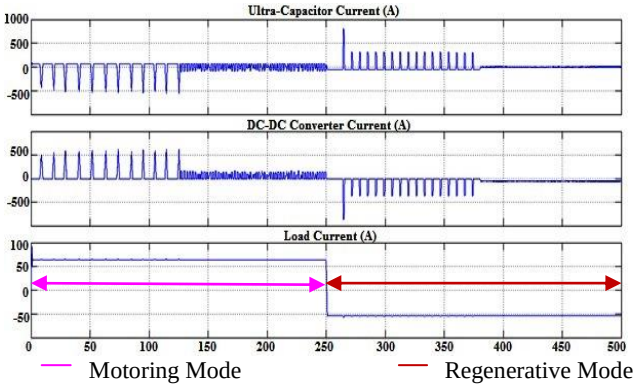

Fig. 24: Simulation Results for Combined Mode with Variable Window. From Top: Ultra-Capacitor Current, DC-DC Converter Current and Load Current

From 0-125 sec, the capacitor voltage is controlled with a larger window. Thus the capacitor is able to discharge its energy into the load from the instant voltage reaches the upper limit. After the capacitor reaches its minimum limit, the energy is supplied by the battery. Thus the battery supplies both the load as well as the capacitor. This mode of operation is not beneficial for the battery which has to supply high peak pulses. From 125-250 sec, the capacitor voltage is confined to a smaller window. As a result, the peak current from the battery has decreased. The next two sections from 125-375 sec and 375-500 sec show the result for regenerative mode with increased and decreased window.

Thus from the simulations it can be seen that by dynamically adjusting the hysteresis window, it is possible to control the charge and discharge rate of the battery.

VII. Summary Of Simulation Results

The power delivered or absorbed by the capacitor for the operating period to support the given load, the influence of hysteresis window and the magnitude of capacitances used are depicted in bar graphs discussed below. Figures 25 to 28 show the plots of output power delivered or absorbed versus time in forward mode and regenerative mode respectively for different values of capacitors.

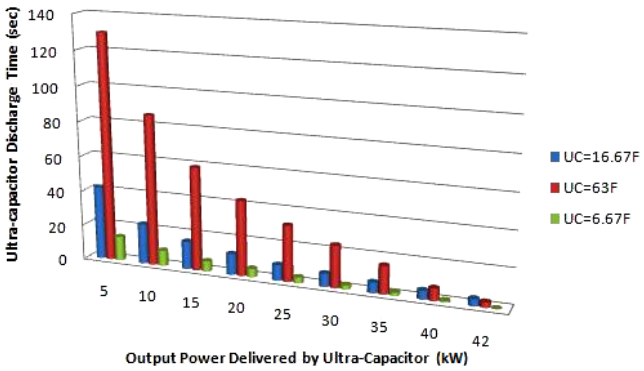

Fig.25: Ultra-Capacitor Output Power Delivered Vs Time for Normal Window of Hysteresis Control

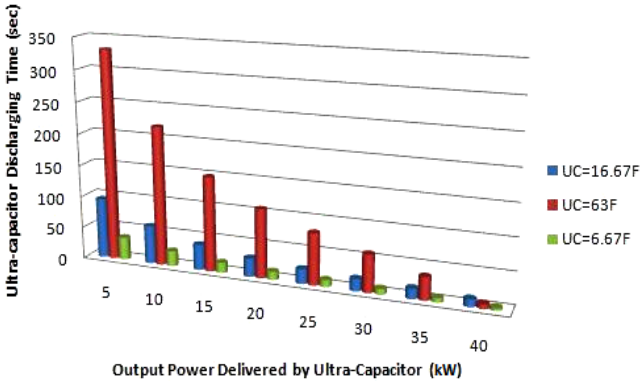

Fig.26: Ultra-Capacitor Output Power Delivered *Vs* Time for Increased Window of Hysteresis Control

Figures 25 and 26 show the plots for the normal (450V-480V) and increased (400V-480V) hysteresis control bands. Different capacitor ratings of 6.67 F, 16.67F and 63F are considered for the study. For normal window, it can be seen that the capacitor with large rating of 63F is able to deliver a large burst of 30-40kW quite amicably for almost 10-20 sec as against 4-8 sec from the smaller capacitors. As expected from the studies made in the previous sections, the increased window causes the capacitors to discharge more power into the load compared with the normal window. Hence, when burst of power is needed for acceleration, the window may be increased by lowering the lowest threshold.

Similarly the increased window allows the capacitor to discharge deeper such that the power demand is met for a sustained period of 20-50 sec.

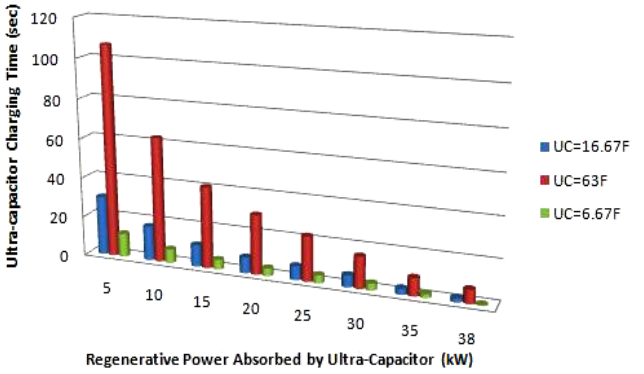

Fig.27: Regenerative Power Absorbed by Ultra-Capacitor *Vs* Time for Normal Window of Hysteresis Control

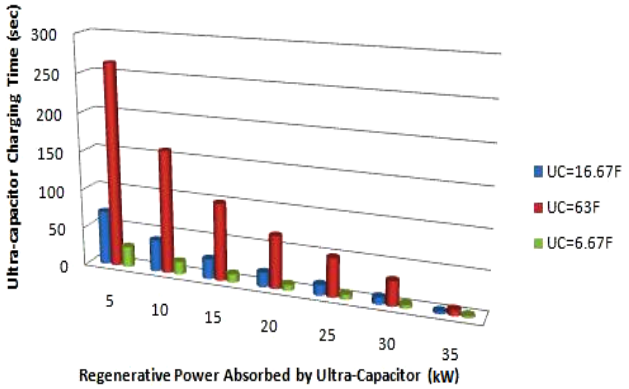

Fig.28: Regenerative Power Absorbed by Ultra-Capacitor Vs Time for Increased Window of Hysteresis Control

The regenerative power absorbed versus time plots for normal (480V-500V) and increased window (480V-500V) are shown in Fig. 27 and 28 respectively. The plots confirm that the energy stored is directly proportional to the value of the capacitor as well as the window width. The study shows that by proper selection of window size and capacitor, the battery can be protected against sudden bursts of regenerative power. Through the plots one can select appropriate windows and capacitor so as to absorb or deliver the required energy.

VIII. Concluding Remarks

In the present simulation study, the impact of hysteresis window on the performance of a hybrid system wherein the ultra-capacitor, fed by a bidirectional converter directly connected across the load is discussed. The simulation study was mainly carried out for various cases in the forward as well as regenerative modes of the motor load pertaining to different capacitances and different hysteresis windows. From the simulation results it can be seen that the smaller hysteresis window will prevent frequent charge-discharge cycles of the capacitor and does not allow the capacitor to deliver or absorb sudden thrust of power. On the other hand, the larger hysteresis window causes charge-discharge cycles but permits discharging of capacitor to meet the sudden demand. Thus the load seen by the battery during forward and regenerative mode can be controlled by controlling the hysteresis window. Hence there is a need for a variable window controller that will adjust not only the window but also the upper and lower limits in accordance with the modes of operation. In all the previous literatures, there is no discussion on varying the upper and lower limits of the hysteresis band. The simulation study clearly depicts that the energy management of ultra-capacitor is very vital for the operation. The present paper has shown that the capacitor energy can be better managed by making the upper and lower limits variable depending on the operating modes. The paper has thoroughly analyzed the variable window control supplemented by the model of the bidirectional topology. The simulation study helps in the selection of the capacitor and the hysteresis band.

IX. Future Work

In the battery/ultra-capacitor HESS configuration discussed above, a control mechanism needs to be

implemented which according to the speed of operation during either acceleration or deceleration should be able to maintain the charge on the ultra-capacitor for supplying variable load or absorbing the regenerative power for charging the battery. Hence a variable window of the hysteresis control is desired which according to the load requirements and the mode of operation can automatically shift the lower threshold limit of the capacitor voltage conveniently.

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Hardware Enactment for Sagacious Compensation by Single Phase Dynamic Voltage Restorer

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Abstract–This paper discusses the hardware implementation of single phase dynamic voltage restorer for the mitigation of voltage sag. The contribution of dynamic voltage restorer for mitigation of voltage sag is first tested by simulation in PSCAD software. The simulated results are validated by an experimental prototype in laboratory. A low power dynamic voltage restorer is built for experimental verification. d-SPACE RTI-d1104, is used for providing gating pulses to the inverter in DVR. Dynamic voltage restorer is implemented for mitigating the sag in open loop control mode as well as close loop control mode. Selected experimental results are reported with analytical findings which show the effectiveness of proposed dynamic voltage restorer for voltage sag mitigation. The proposed DVR is also able to keep total harmonic distortions of load voltage within permissible THD voltage limit.

Keywords–Dynamic voltage restorer (DVR), voltage sag, sinusoidal pulse width modulation (SPWM), power quality, total harmonic distortion (THD).

I. INTRODUCTION

Power quality issues are one of the major concerns in this modern era of industrial power consumer. It is due to increase use of sensitive and critical equipments in the system such as communication system, process industries precise manufacturing process etc. Among the entire power quality disturbances, voltage sag is most common and frequently occurring phenomenon in distribution system [1]. In electrical grid system it is not possible to avoid voltage sag because of finite clearing time of faults that cause the voltage sag and propagation of sags from the transmission and distribution system to the low voltage load. Voltage sag is the common reasons for interruption in production plants and for end user equipment malfunction in general. Most of the research work is concentrated on voltage sag analysis and its mitigation [2].

In order to overcome this problem, the concept of custom power devices is introduced [3-4]. Custom power devices are mainly of three categories such as series connected compensator i.e. dynamic voltage restorer (DVR), shunt connected compensator (DSTATCOM) and a combination of series and shunt connected compensator known as unified power quality conditioner (UPQC). Among all these DVR is found to be a cost effective solution for voltage sag mitigation [5]. The DVR can regulate the load voltage from the problems such as sag, swell and harmonics in the supply voltage. Hence, it can protect the critical consumer loads from tripping and consequent losses. Implementation of the DVR have been proposed at a low voltage (LV) level as well as a medium voltage (MV) level and serves to protect the high power sensitive loads from voltage sags. DVR is made up of solid state switching devices. It is power converter that injects the a.c. voltage in series and synchronism with the distribution feeder voltage. The amplitude and phase angle of injected voltages are variable, thereby allowing control of real and reactive power exchange between the DVR and distribution system.

In this research work, a single phase DVR operation for voltage sag mitigation in open loop as well as close loop is presented. To verify theoretical performance, the simulation is carried out in PSCAD software and then hardware prototype model of DVR is developed in laboratory. d-SPACE RTI-d1104 is used for providing the gate pulses in open loop as well as close loop control modes. Finally simulation results followed by experimental results are presented.

This paper is organized as: Principle operation of DVR is explained in section II. The details of compensation technique which is used for sag mitigation is discussed in section III. The simulated and experimental results for open loop and closed loop control of DVR are illustrated in section IV. The conclusion is given in section V.

II. PRINCIPLE OF OPERATION OF DVR

The schematic diagram of a typical single phase DVR used for voltage correction is shown in Fig. 1. The DVR consist of voltage source converter, an injection transformer, passive filter and energy storage [6-7]. In this research work rectifier is used for D.C. link. When the supply voltage V_s changes, the DVR injects a voltage V_{inj} in such a way that the desired load voltage magnitude can be maintained. The DVR is simply a voltage source inverter that produces an ac output voltage and injects in series with supply voltage through injection transformer. Fig. 2 shows the equivalent diagram of DVR and principle of series injection for voltage sag compensation. From Figs. 1, 2 and 3 neglecting Z_{line} and Z_{dvr}

$$\vec{V}_L = \vec{V}_s + \vec{V}_{inj} \quad (1)$$

where $\vec{V}_L$ is load voltage, $\vec{V}_s$ is supply voltage and $\vec{V}_{inj}$ is the injected voltage by DVR. Depending on the injection control scheme used, explained in section 3 the injected voltage of DVR can be calculated using equation (1).

III. COMPENSATION TECHNIQUE FOR DVR

Voltage injection or compensation methods by means of a DVR depend upon the factors such as; DVR power rating, various conditions of load and different types of voltage sag. Some loads are sensitive towards phase angel jump, some are sensitive towards change in magnitude and others are tolerant to these. Therefore the control strategies depend upon the type of load characteristics. There are different methods of DVR voltage injection [5], [8-10] which are

- In-phase compensation method

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- Pre-sag compensation method
- Phase advanced compensation method

A. In-Phase Compensation

In this method, the DVR voltage is injected in phase with the supply voltage [10]. When the load voltage drops due to sag, DVR will inject voltage depending on the dropped voltage magnitude in phase with the sag voltage regardless of load current and pre-sag voltage. Thus for load terminal, voltage during sag and pre-sag is same. This is the simplest way to mitigate voltage sag without phase angle jump. The advantage of this method is that the magnitude of injected DVR voltage is minimized for constant load voltage magnitude. Because in this method the load voltage is algebraic sum of sag voltage and injected voltage. For compensating the sag with phase angle jump generally pre-sag compensation technique is used.

Fig. 3 shows the phasor diagram of different voltage injection schemes of DVR. $V_{L(pre\text{-}sag)}$ is a voltage across the critical load prior to the voltage sag condition. During the sag condition supply voltage is reduced to V_{sag} with angle θ. Now, the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. V_{inj1} in Fig. 3 represents the voltage injected in phase with supply voltage.

B. Pre-Sag Compensation

The pre-sag compensation method tracks the supply voltage continuously and compensates load voltage during sag to restore the pre-sag condition. V_{inj2} in Fig. 3 shows the single-phase vector diagram of the pre-sag compensation. In this method the injected active power cannot be controlled and it is determined by external conditions such as type fault and load conditions. The injected voltage requirement is more compared to in-phase injection scheme.

C. Phase-Advanced Compensation

In pre-sag compensation and in-phase compensation methods the DVR must inject the active power to the load almost all the time. But in phase advanced compensation the injected voltage phasor is perpendicular to load current phasor, because of which active power supplied by DVR is zero. V_{inj3} in Fig. 3 represents the phase advanced compensation. Injection voltage magnitude is larger in phase advanced compensation as compared to pre-sag and in- phase compensation. But all the sags cannot be restored without real power; as a consequence, this method is only suitable for a limited range of sag.

From the phasor diagram shown in Fig. 3 it is clear that a minimum possible rating of converter is achieved with in-phase injection scheme. So in this paper, in-phase compensation control scheme for DVR is implemented to reduce the rating of DVR. In in-phase compensation method th**e** rating of DVR can be given as [8]

$$S_{DVR} = V_{DVR} \times I_L^* \quad (2)$$

$$I_L = \frac{(P_L + jQ_L)}{V_L} \quad (3)$$

For this research work sensitive load is resistive load

$$S_{DVR} = V_{DVR} \times I_{DVR} \quad (4)$$

where

$$I_{DVR} = I_L \quad (5)$$

V_{DVR} is the maximum voltage injected by the DVR in phase with supply voltage and I_L is the load current. The active power consumption of DVR should not exceed a certain value, since it increases the power rating of DVR. If the injected voltage of DVR exceeds a certain value, the active power consumption of the DVR violates the power limit. Hence the maximum injection of DVR voltage should not go beyond a value 0.5 *p.u.* Hence the maximum voltage injected by DVR is 50 % of supply voltage.

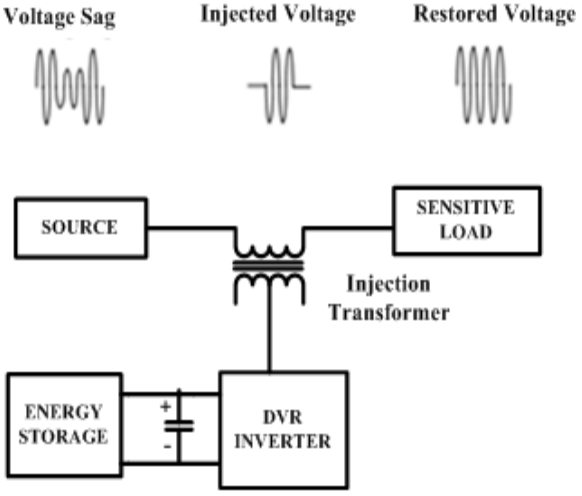

Fig. 1: Schematic diagram of DVR

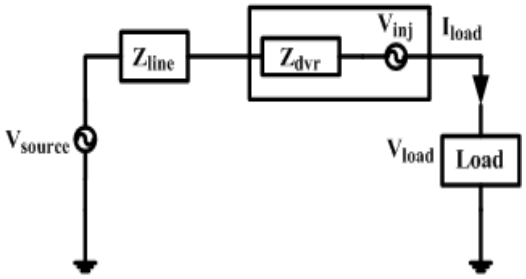

Fig. 2: Single phase equivalent circuit of DVR

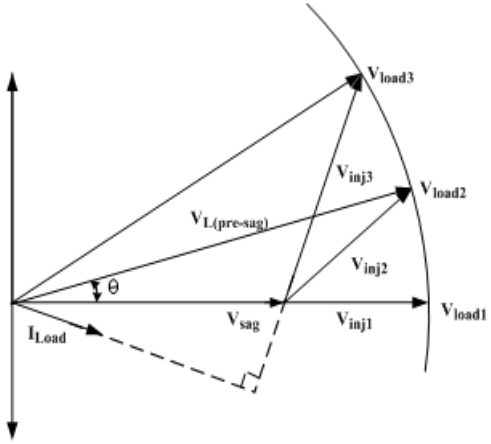

Fig. 3: Phasor diagram of DVR voltage injection scheme

IV. Simulated and Hardware Results

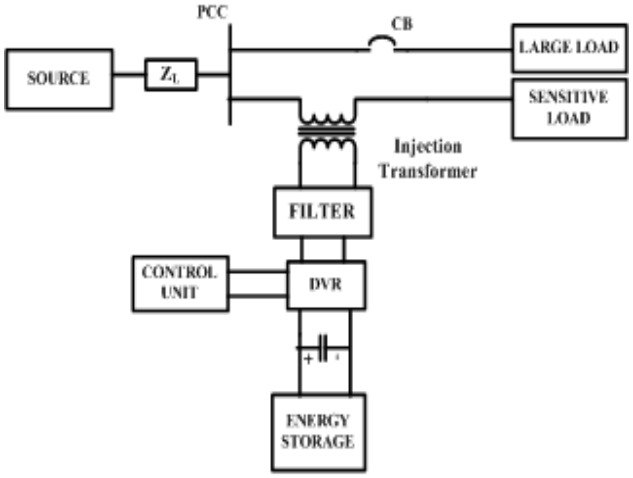

Fig. 4: Study case

A. Open Loop Performance

Fig. 4 shows the test system under consideration to carry out the transient modeling of DVR for software and hardware analysis [11]. The test system comprises of 115 volt a.c. transmission systems. A heavy load is connected at the PCC through circuit breaker which is in parallel with the sensitive load. A single phase VSI based DVR is connected in series with the sensitive load to provide instantaneous voltage support at the load point and during voltage sag. The voltage sag is occurred at PCC and load points due to sudden switching of heavy load due to presence of source and transmission line impedance.

a. Simulation Result

The above study case is first simulated in PSCAD for open loop control of DVR. The system parameters for simulation and hardware are given in Table 1. Fig. 5 shows the study case implemented in PSCAD. The sag is created by switching on heavy load during a period of 0.3 to 0.6 sec. Fig. 6 shows the waveform of source voltage and load voltage without DVR. The source voltage is 162 V peak to peak. The pre-sag load voltage is 155 V peak to peak and during sag it reduced to 122 V. The PCC and load voltage will experience sag but source voltage remains unaffected. Fig. 7 shows the rms value of source voltage and load voltage without DVR. The source voltage is 115 V, and the load voltage without sag is 110 V and during sag is 88 V. It is seen that the voltage at load point experiences the sag of 22 V with respect to pre-sag load voltage

At the point of sag, DVR is turned on. The load voltage during sag is measured and compared it with the reference voltage and generated as an error signal to operate the VSI to produce the required voltage, which is injected in series with sag voltage i.e. nothing but the PCC voltage in this case to mitigate the sag. Fig. 8 shows the instantaneous waveform of source and load voltage with DVR. The output of DVR which is injected is without filter. Fig. 9 shows rms value of source and load voltage with DVR. From the Fig. 9, it is clear that the load voltage is maintained constant to pre-sag value of 110 V with the operation of DVR.

Table 1: System parameters

Parameter	Specification
Source Voltage	115V
Load Voltage	110 V
Sensitive Load	40 W
Heavy load	1000 W
Switching Frequency	1 kHz
Injection Transformer	110/110 V, 1 kVA
Filter Inductance	10 mH
Filter capacitor	105 µF, 250 V
Transmission line impedance	3 Ω

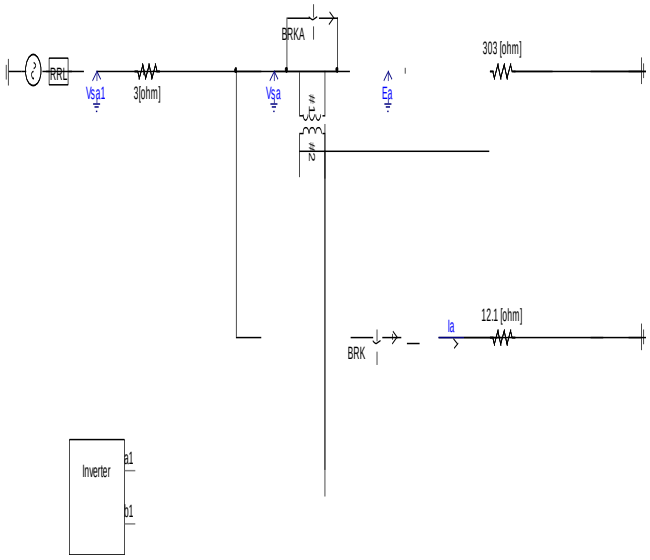

Fig.5: Test system implemented in PSCAD

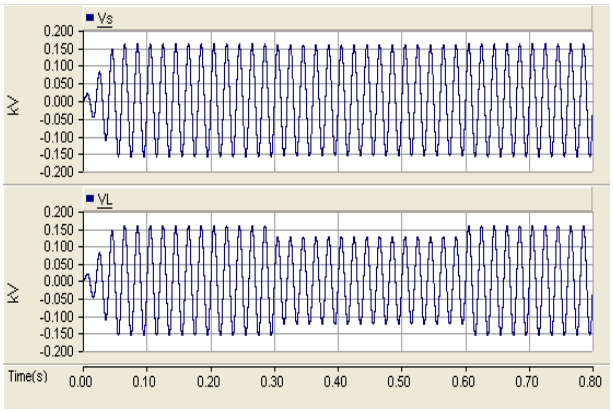

Fig. 6: V_s- source voltage and V_L- load voltage without DVR

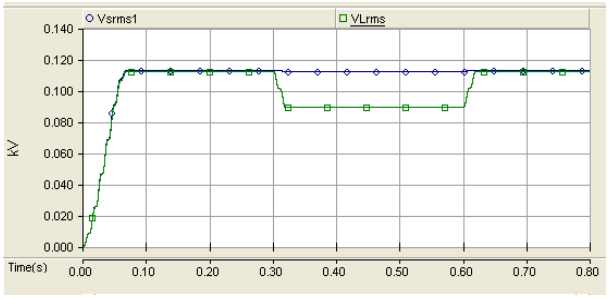

Fig. 7: RMS value of V_s- source voltage and V_L-load voltage without DVR

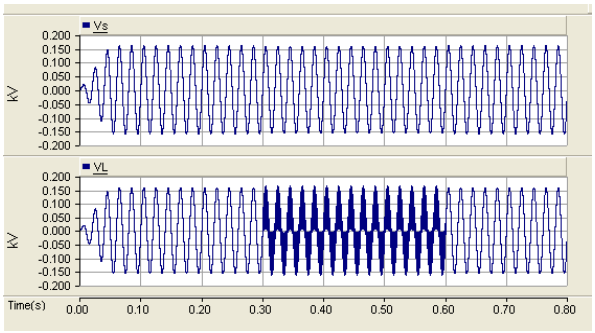

Fig.8: V_s- source voltage and V_L-load voltage with DVR

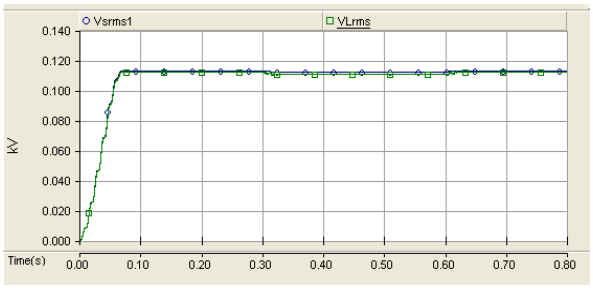

Fig. 9: RMS value of V_s-source voltage and V_L-load voltage with DVR

b. Experimental Results

A real time hardware set up has been implemented to explore the function of DVR to mitigate the voltage sag. The complete hardware setup circuitry of DVR is shown in Fig. 10. It shows the source, sensitive load, heavy load, injection transformer, LC filter of DVR and d-SPACE RTI d-1104. The MOSFET IRF460 is used as switches for power circuitry of voltage source inverter. Gate driver IC MIC4425, Opto-coupler 6N137 and buffer IC 74Ls07 are used for gate driver circuit. Voltage sensors are used to sense the load voltage and reference voltage.

Intentionally sag has been induced by switching on a heavy load suddenly, which is connected in parallel to the sensitive load at PCC. DVR is connected in series with the sensitive load and gate pulses provided for the inverter through d-SPACE system. The load voltage is continuously measured by using voltage sensor. A differential probe has been used with a multiplying factor of '20X' for every measurement throughout the tenure of the project. The experimental waveforms of source voltage, load voltage, injected voltage and inverter output voltage without DVR operation are shown in Fig. 11. The source voltage is 16 *V* peak to peak (i.e. *rms* 115 *V*) is shown in channel 1. The load voltage is shown in channel 2, pre-sag load voltage is 15.6 $V_{p\text{-}p}$ (i.e. 110 V_{rms}) and during sag it dips to 88 V_{rms}. The voltage across DVR is shown in channel 3 and across inverter is shown in channel 4. It is observed that the voltage across the inverter is zero since no gate pulses have been provided to the inverter; that is DVR is not injecting the voltage.

Fig. 12 shows all above four voltage waveforms when DVR is injecting the voltage in open loop. Point A on channel 2 of Fig. 12 indicates the occurrence of sag due to switching on heavy load which dips the sensitive load voltage to 88 V_{rms} value. It means that sag has occurred by 22 V_{rms}. Now the contribution of DVR comes into picture. Area B indicates the time period when DVR is in operation. Channel 3 shows the injected voltage of DVR which is 22 V_{rms}. So it is observed that load voltage has been recovered to 110 V_{rms} with injection of DVR voltage. The point C shows the time when DVR is turned OFF. To have a clear understanding regarding the operation of DVR, the sag is continued even after point C. Channel 4 shows the inverter output voltage during operation of DVR. The DVR output is filtered and then it is injected to the supply voltage i.e. PCC voltage to carry out in phase injection. THD analysis of load voltage after injecting the voltage through DVR is carried out for open loop condition and it is as shown in Fig. 13. The THD of load voltage during DVR operation is 4.22%, which is within permissible limit. The comparison of source and load voltage during sag and pre-sag condition for open loop system is given in Table 2.

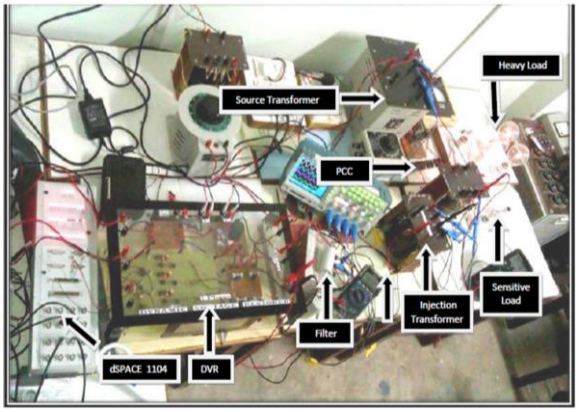

Fig.10: Complete hardware setup for DVR operation

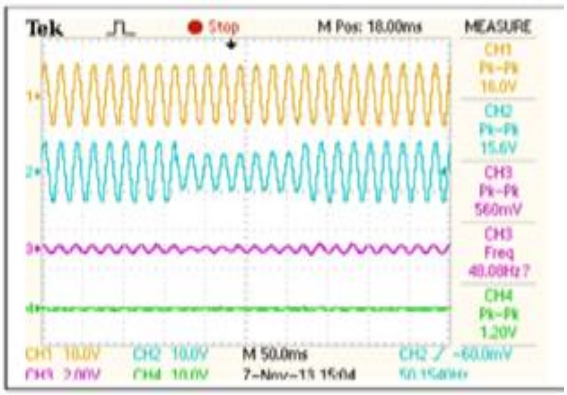

Fig. 11: Experimental waveforms without DVR Ch.1- source voltage, Ch.2- load voltage, Ch.3- injected voltage and Ch.4- voltage across inverter

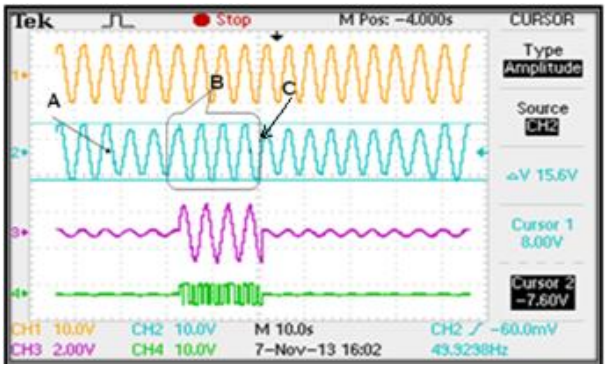

Fig. 12: Experimental waveforms with DVR Ch.1- source voltage, Ch.2 -load voltage Ch. 3- injected voltage and Ch. 4- inverter output voltage

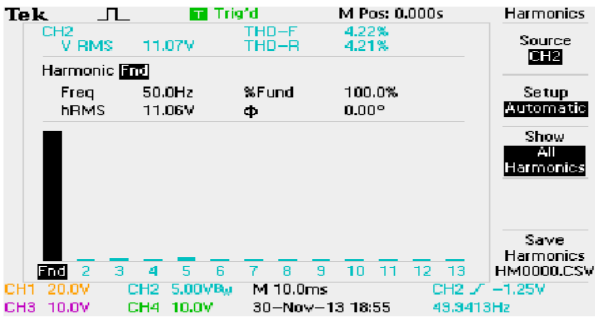

Fig. 13: Harmonic spectrum of load voltage

Table 2: Comparison of different voltages

Measured Voltage (Peak–Peak)	RMS Voltage
Vs = 16.0	115 V
V_L= 15.6	110 V (pre-sag voltage)
V_L= 12.4	88 V (During sag without DVR injection)
Sag Voltage =3.2	22 V (drop in voltage)
DVR = 3.2	22 V (injected voltage)
V_L= 15.5	110 V (with DVR)

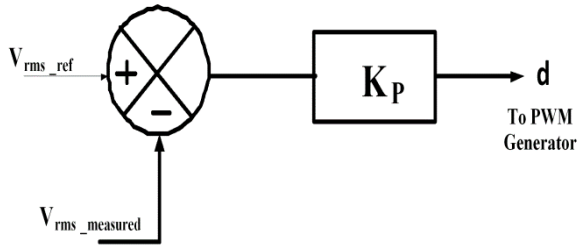

Fig. 14: Basic control scheme for DVR

B. Closed loop Performance

a. Simulation Results

A block diagram for control scheme for DVR is shown in Fig. 14. P controller is used in this research work as it is simple to design. It is based on measurements of the *rms* voltage (V_{rms}) at the load point. The voltage error signal is obtained by comparing measured V_{rms} against reference voltage, $V_{rms\text{-}ref}$ [12-13]. The difference between these two signals is processed by P controller, and the P-controller output is use to generate the pulses through PWM generator for triggering voltage source inverter. The value of K_p is calculated to keep the error minimum and to maintain modulation index 0.8.

For better observation the source voltage is increased to 125 V (i.e. 177 V_{peak}). The load voltage without sag is 123V (i.e.174 V_{peak}). Dip sag has been created by connecting heavy load during 0.3 to 0.6 s. The load voltage dips to 88 V_{rms} (i.e.121 V_{peak}). Fig. 15 shows the waveforms of load voltage without and with DVR. The *rms* value of source and load voltage with DVR is shown in Fig. 16. From Fig. 15 and 16 it is clear that with the operation of DVR value of load voltage is also restored to its pre-sag value.

b. Experimental Results

Fig. 17 shows the source and load voltage without DVR in close loop operation. Channel 1 shows 17.6 $V_{p\text{-}p}$ (i.e. 125 V_{rms}). Channel 2 shows the load voltage. Voltage across the load under pre-sag condition is 17.5 V (i.e.123 V_{rms}). When the heavy load is suddenly switched on sensitive load voltage is suddenly dips to 85 V_{rms}. It means that sag has been occurred for 39 V_{rms}. Fig. 18 shows the source voltage (Channel 1), load voltage (Channel 2) and injected voltage of DVR (Channel 3) during DVR operation. Point A on waveform 2 indicates the occurrence of sag. Area B indicates the time period of operation of DVR. The injected voltage of 36 V_{rms} by DVR has been observed in channel 3. The load voltage is maintained nearly constant as that of pre-sag value during the sag condition the comparison of load voltage during pre-sag and sag condition is given in Table 3.

The THD analysis of the load voltage during DVR operation is carried out as shown in Fig. 19. The THD value is 3.79% which is slightly reduced as compared to THD in open loop. Thus the DVR maintain the sensitive load voltage during sag condition with low THD.

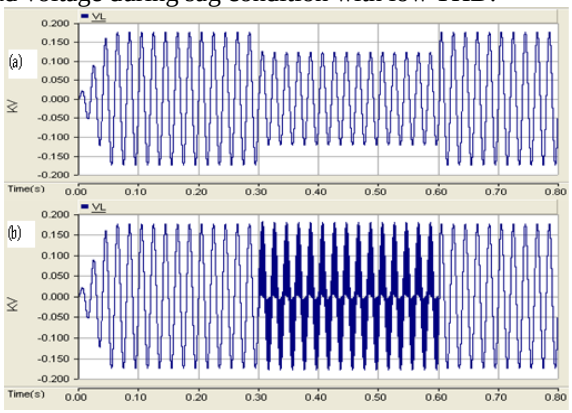

Fig. 15: (a) load voltage without DVR (b) load voltage with DVR

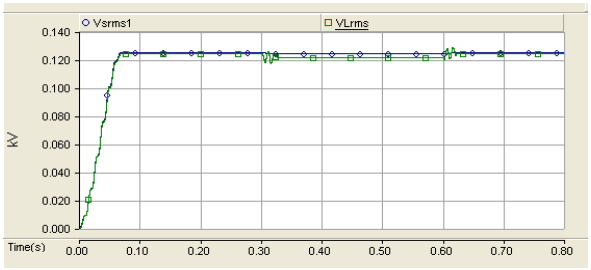

Fig. 16: RMS value of V_s- source voltage and V_L- load voltage with DVR

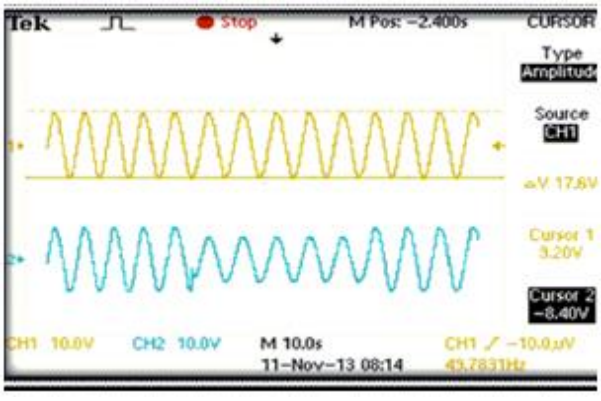

Fig. 17: Experimental waveforms without DVR Ch.1- source voltage Ch.2 -load voltage

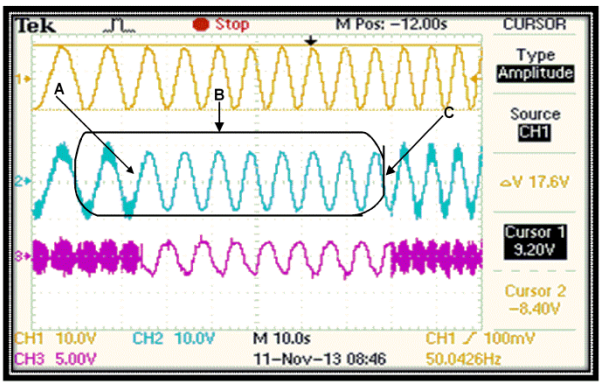

Fig.18: Experimental waveforms with DVR Ch.1 source voltage, Ch. 2 -load voltage and Ch.3- injected voltage

Table 3: Comparison of different voltage

Measured Voltage ($V_{p\text{-}p}$)	RMS (Volts)
V_s = 17.6	125
V_L= 17.5	123 (Pre-sag)
V_L= 12.0	85 (during sag)
Sag = 5.6 $V_{p\text{-}p}$	39 (drop in voltage)
DVR injection = 5	36 (injected voltage)
V_L=17.2	121(with DVR)

Fig. 19**:** Harmonic Spectrum of load voltage under close loop operation

V. CONCLUSION

VSC based single-phase DVR is lighter, cheaper and expandable to multilevel version to enhance the performance with lower switching frequency and it is popular in UPS based application. In this research work capability of single phase VSC based DVR for voltage sag mitigation in open loop as well as close loop is tested by actual prototype of DVR for study case. The operation of DVR is demonstrated in in-phase injection control scheme to reduce the rating of DVR. The simulation of DVR for mitigation of voltage sag is first carried out in PSCAD software. The simulated results are confirmed by experimental results. From the results, it is observed that the proposed DVR mitigates the voltage sag. It is found that the THD of sensitive load voltage is within permissible limit with the use of DVR under both open loop as well as close loop control.

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